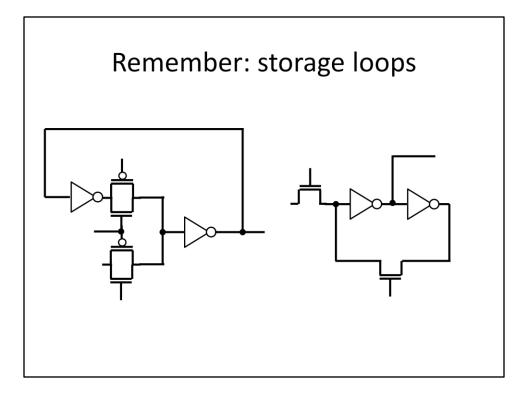


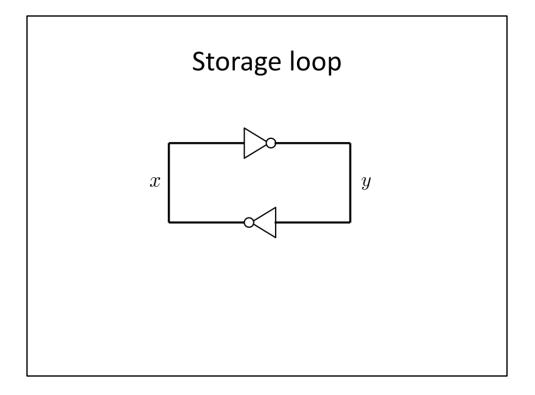
Metastability

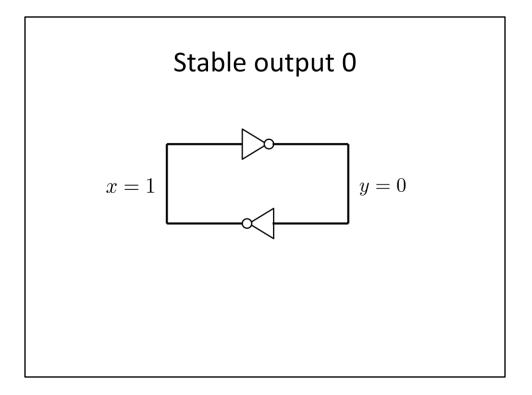
storage element:

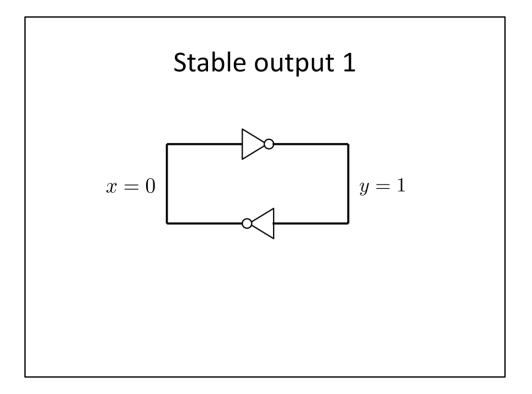
can store stable 0 & 1

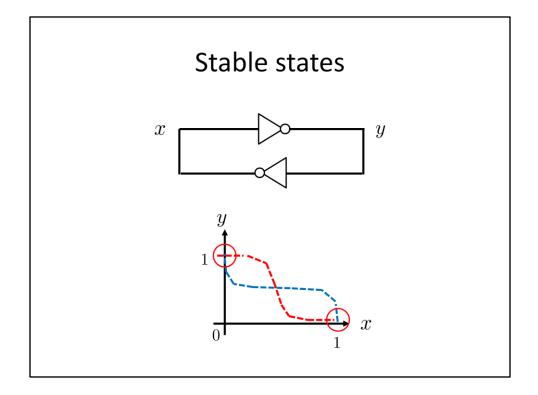
potentially also stores a third metastable state



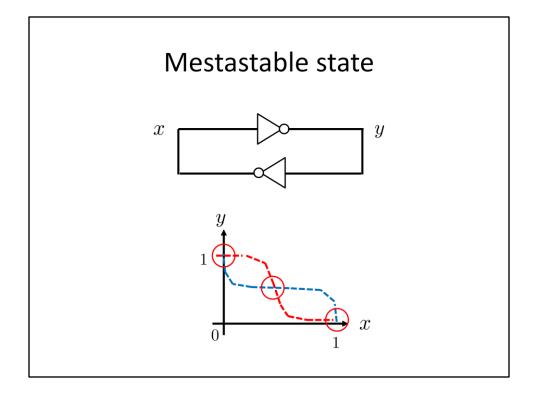






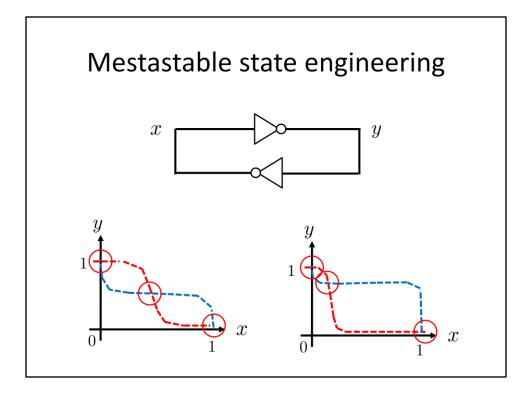


below: input-output voltage after transient effects decayed

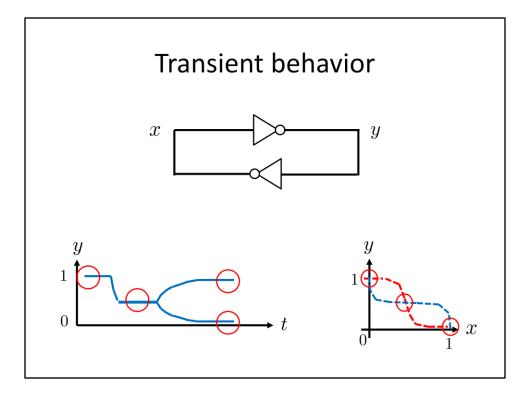


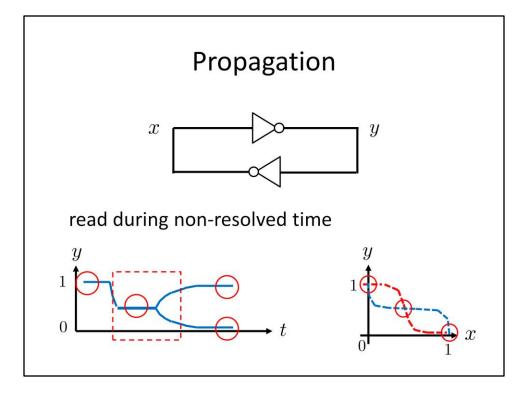
Third state also solves the steady state equations of both inverters.

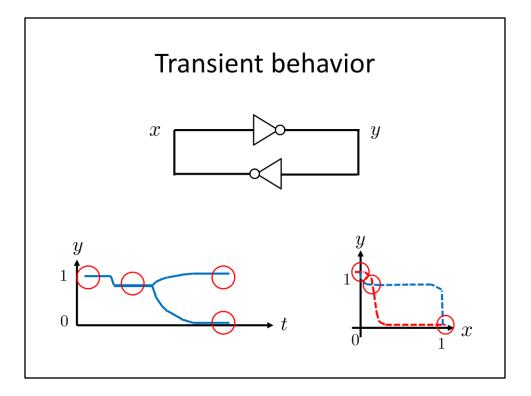
However, "metastable": small disturbance makes it resolve to a stable 0 or 1 state.

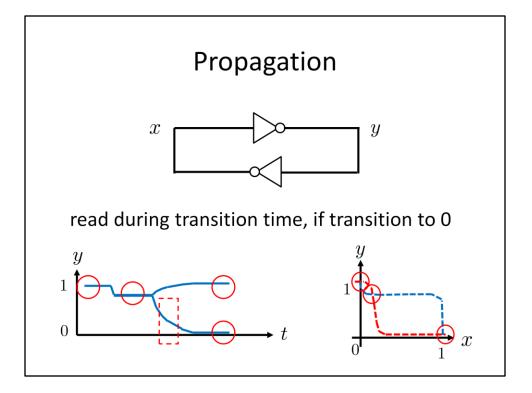


low & high threshold inverters to shift metastable state to a region that is well recognized as 1 (here) or 0 when read.





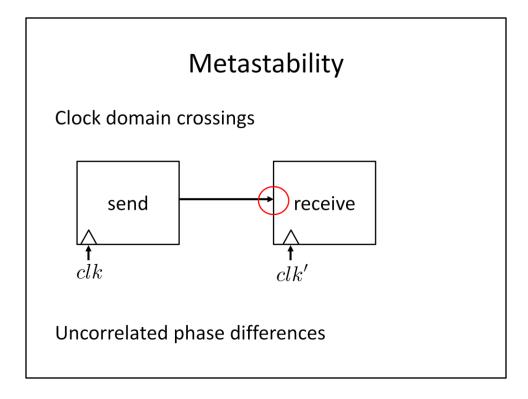


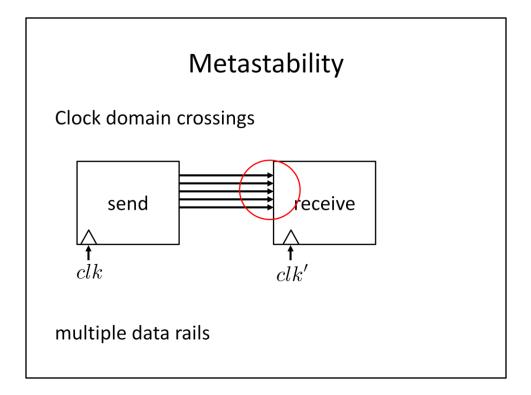


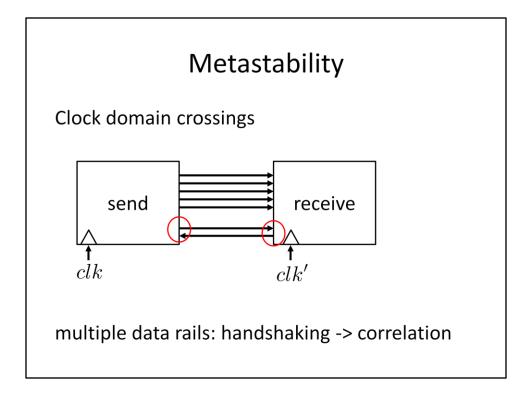
Metastability

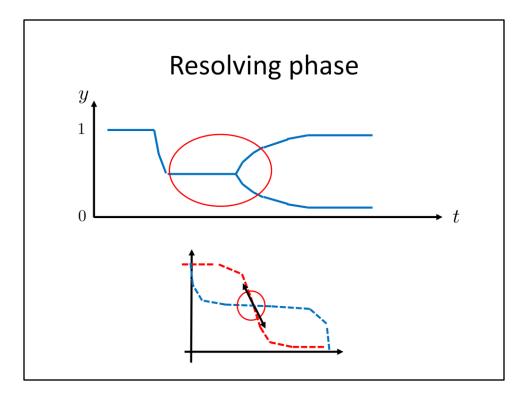
causes:

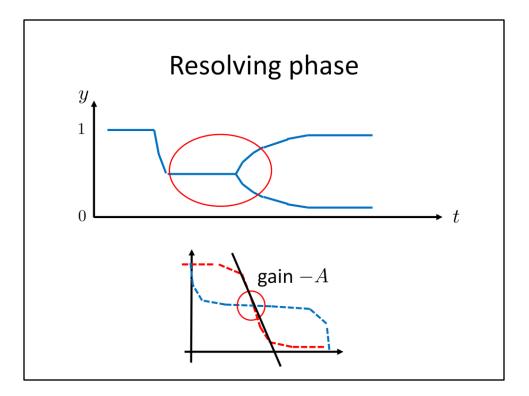
- violation of setup/hold times
- induced by faults (e.g. particle hits)

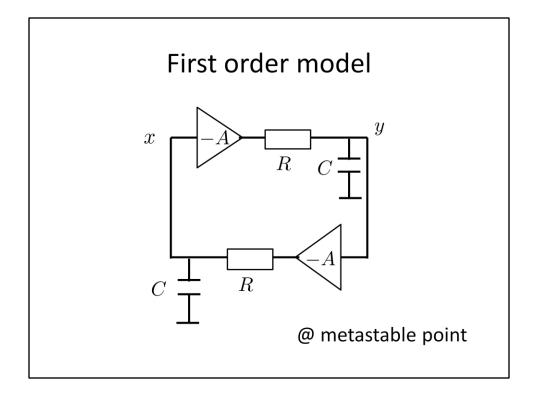






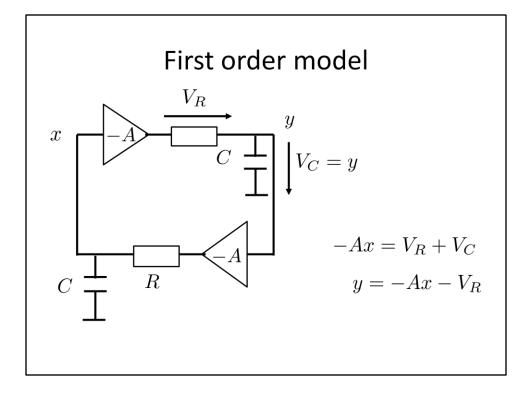


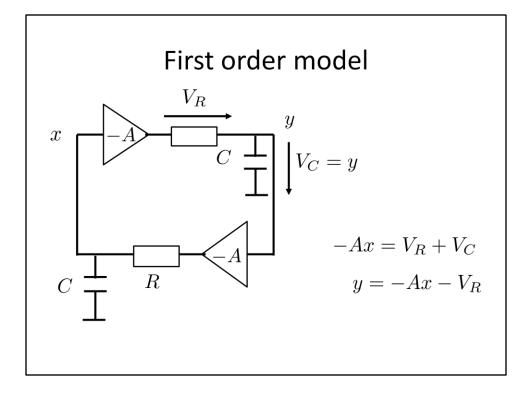


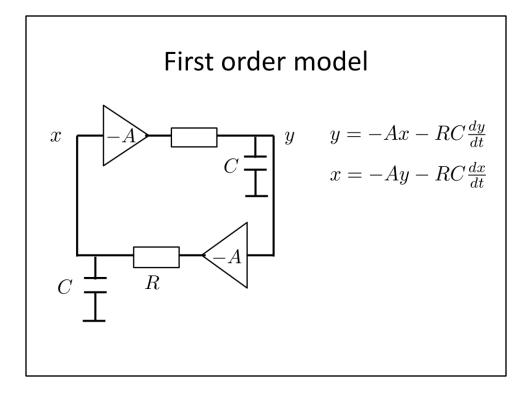


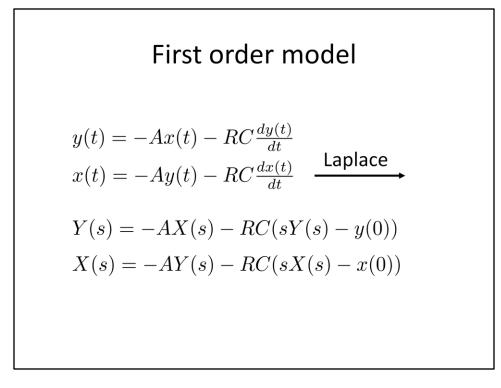
gain –A, first order RC model.

Here: assume that both inverters same characteristics









First order model

$$Y(s) = -AX(s) - RC(sY(s) - y(0))$$

$$X(s) = -AY(s) - RC(sX(s) - x(0)) \longrightarrow$$

$$Y = \frac{A^2}{(1+s\tau)^2}Y - \frac{A\tau x(0)}{(1+s\tau)^2} + \frac{\tau y(0)}{1+s\tau} \longrightarrow$$

$$Y(1 - \frac{A^2}{(1+s\tau)^2}) = -\frac{A\tau x(0)}{(1+s\tau)^2} + \frac{\tau y(0)}{1+s\tau}$$

tau = RC

$$First order model$$

$$Y(1 - \frac{A^2}{(1+s\tau)^2}) = -\frac{A\tau x(0)}{(1+s\tau)^2} + \frac{\tau y(0)}{1+s\tau} \longrightarrow$$

$$Y = \frac{1}{2} \left(\frac{y(0) - x(0)}{-(\frac{A-1}{\tau} + s)} + \frac{y(0) + x(0)}{-(-\frac{A+1}{\tau} + s)} \right) \xrightarrow{\text{inv Laplace}}$$

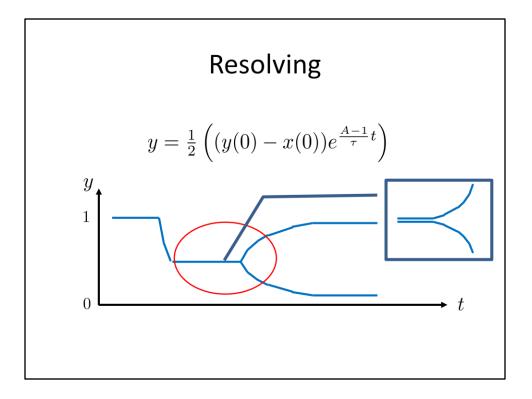
$$y = \frac{1}{2} \left((y(0) - x(0))e^{\frac{A-1}{\tau}t} + (y(0) + x(0))e^{-\frac{A+1}{\tau}t} \right)$$

First order model

$$Y(1 - \frac{A^2}{(1+s\tau)^2}) = -\frac{A\tau x(0)}{(1+s\tau)^2} + \frac{\tau y(0)}{1+s\tau} \longrightarrow$$

$$Y = \frac{1}{2} \left(\frac{y(0) - x(0)}{-(\frac{A-1}{\tau} + s)} + \frac{y(0) + x(0)}{-(-\frac{A+1}{\tau} + s)} \right) \xrightarrow{\text{inv Laplace}}$$

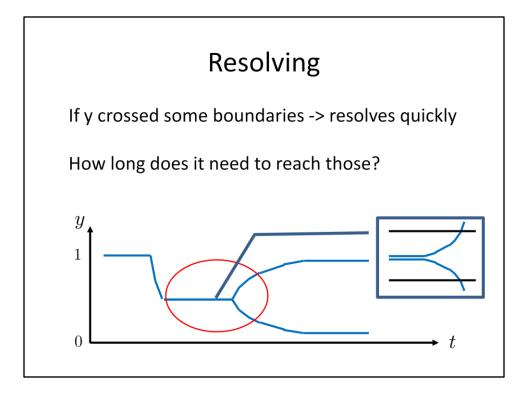
$$y = \frac{1}{2} \left((y(0) - x(0))e^{\frac{A-1}{\tau}t} + (y(0) + x(0))e^{-\frac{A+1}{\tau}t} \right)$$
...dominant term

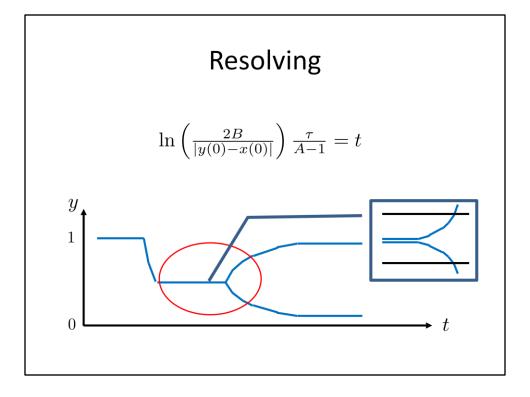


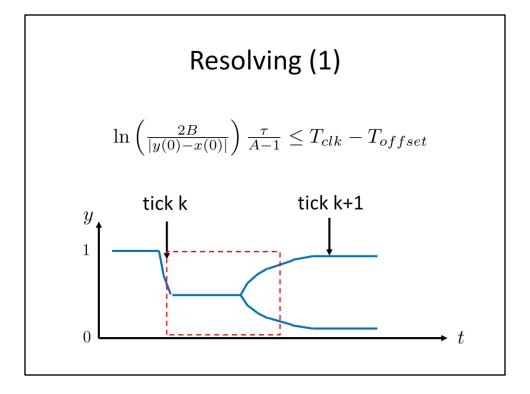
mind: the above equation only holds near the metastability point.

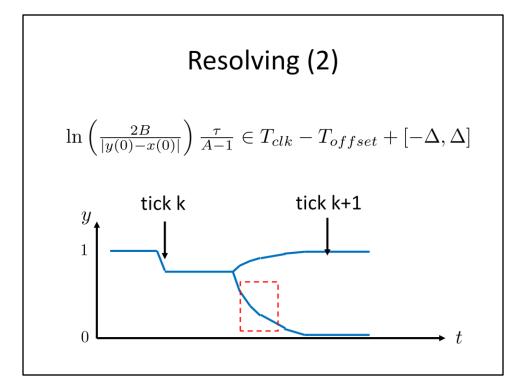
it assumes e.g. that gain A is constant and not depenent on the input voltages x or y of the inverters.

gain is different (around 0) for points near stable 0 or 1.









Resolving

y(0) - x(0)

Depends on phase relation of input change to clock transition.

Several model assumptions to quantify it.

Literature: typically exponentially/uniformly distributed input changes & linear change over time.

MTBU

upset [here, (1)]: if metastability resolves after next tick

MTBU $\propto e^{\frac{A-1}{\tau}(T_{clk}-T_{offset})}$

increase T_{clk} by stacking flip-flops -> synchronizer chains

meantime between upset: expected meantime between two upsets (= not resolved at next clock tick)

MTBU

upset [alternative, (2)]: if metastability resolves **around** next tick

better, but still:

MTBU $\propto e^{\frac{A-1}{\tau}(T_{clk}-T_{offset})}$

Impossibility Result

Marino: "General theory of metastable operation", 1981.

Thm. Any bistable element must have executions with arbitrarily long delays until a stable 0 or 1 state is reached.

Impossibility Result

System model: differential equation on continuous system space.

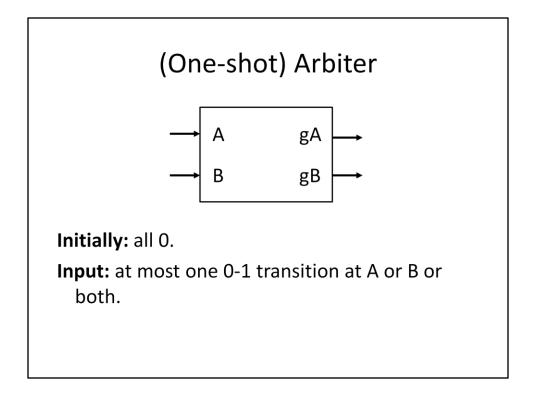
Proof idea: topological.

- 0 & 1 bounded time attractors disconnected regions in system space.
- executions: continuous traces in system space.
- -> must cross non-attractor region

Impossibility Result

Implies impossibility of metastability-free bistable elements by reduction:

arbiter, inertial delay, flip-flop, latch, C-Element, etc.



Arbiter Properties

Mutex. Either gA makes 0-1 transition or gB but never both.

Bounded Time: Output transitions occur at most T1 time after the first input transition.

Validity. If A/B transition at least T2 time before B/A transition -> gA/gB transition occurs