Beyond classical circuit design lecture 6

Synthesis

Further Reading

Alain J. Martin: *Synthesis of Asynchronous VLSI Circuits.* Tech report California Institute of Technology, 1991.

Alain J. Martin and Mika Nyström: *Asynchronous techniques for system-on-chip design.* Proceedings of the IEEE Volume 94, Issue 6:1089 - 1120, June 2006.

Edmund M. Clarke, Orna Grumberg and Doron Peled: *Model Checking.* MIT Press, 1999.

What we had...

- Bare Handshakes -> Communication
- Isochronic fork assumption

- Coming up: Synthesis
  - CSP -> PR
  - PR -> transistors

Synthesis

In: CHP

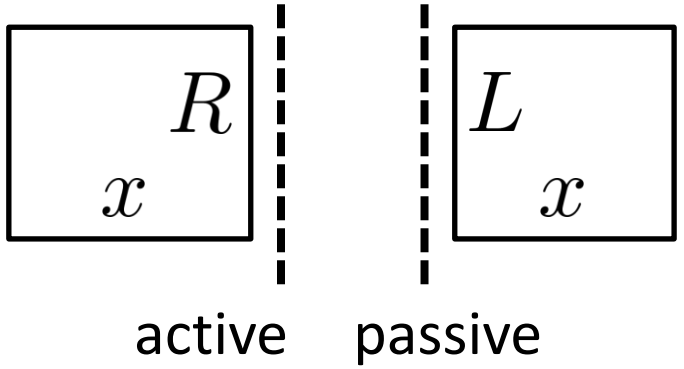
Out: Circuit (= Production rules + constraints)

Example: 1-bit channel

Send $x \in \{0, 1\}$

active send,

passive receive



CHP:

sender: $Ps : *[\ldots R!x \ldots]$

receiver: $Pr : *[\ldots L?x \ldots]$

Example: 1-bit channel

Choice: dual-rail encoding.

$$R!x \quad rd := x; [v(ra)]; rd := neutral; [n(ra)]$$

$$[x \to rd.1 \uparrow || \bar{x} \to rd.0 \uparrow]; [ra];$$
$$(rd.1 \downarrow || rd.0 \downarrow); [r\bar{a}]$$

Example: 1-bit channel

$$L?x \qquad [v(ld)]; y := ld; la\uparrow; [n(ld)]; la\downarrow$$

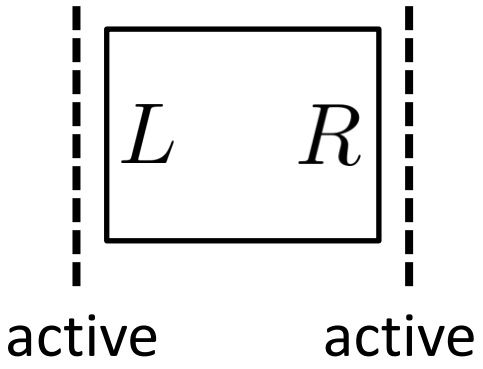
$$[ld.1 \vee ld.0]; [ld.1 \rightarrow x\uparrow \,||\, ld.0 \rightarrow x\downarrow]; la\uparrow;$$
$$[\neg(ld.1 \vee ld.0)]; la\downarrow$$

$$[ld.1 \rightarrow x\uparrow \,||\, ld.0 \rightarrow x\downarrow]; la\uparrow;$$
$$[\neg(ld.1 \vee ld.0)]; la\downarrow$$

Example: active-active sequencer

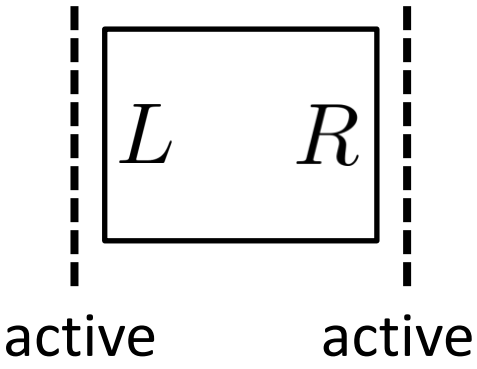
two active interfaces L, R.

CHP: $P1 : *[L; R]$



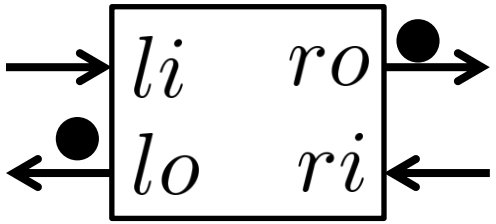
Example: active-active sequencer

two active interfaces L, R.



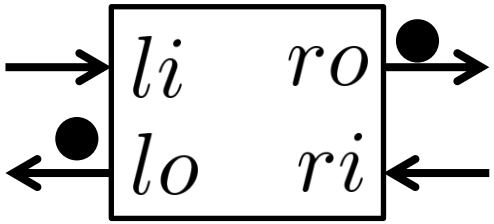
CHP: $P1 : *[L; R]$

Choice: 4-ph hs



$$*[lo\uparrow; [li]; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; ro\downarrow; [\bar{ri}]]$$

For lo…



CHP: $*[lo\uparrow; [li]; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; ro\downarrow; [\bar{ri}]]$

$lo = 0$

by circuit

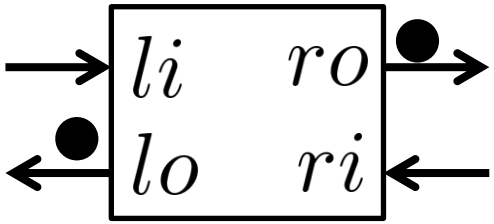
$ro = 0$

$ri = 0$

by environment

$li = 0$

For lo...



CHP: $*[lo\uparrow; [li]; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; ro\downarrow; [\bar{ri}]]$

$lo = 0$

$ro = 0$

by circuit

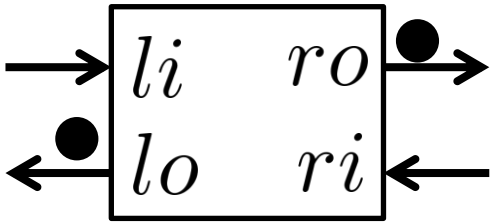
$ri = 0$

$li = 0$

by environment

PR: $\bar{lo} \wedge r\bar{o} \wedge \bar{ri} \wedge \bar{li} \rightarrow lo\uparrow$

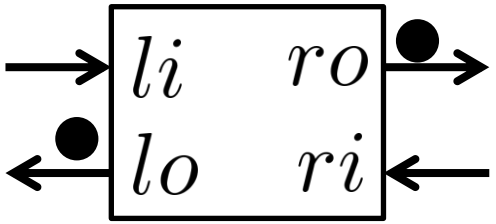
For lo…



CHP: $*[lo\uparrow; [li]; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; ro\downarrow; [\bar{ri}]]$

$$\frac{lo = 0 \quad ro = 0}{ri = 0 \quad li = 0} \qquad \frac{lo = 0 \quad ro = 0}{ri = 0 \quad li = 0}$$

PR: $\bar{lo} \wedge \bar{ro} \wedge \bar{ri} \wedge \bar{li} \rightarrow lo\uparrow$ …. does not work!



CHP: $*[lo\uparrow; [li]; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; ro\downarrow; [\bar{ri}]]$

$x\uparrow$ $x\downarrow$

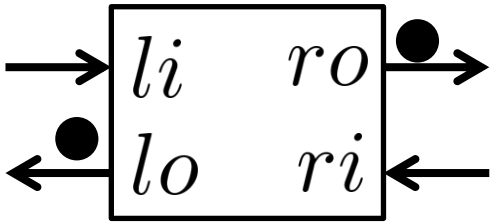
$lo = 0$ $lo = 0$

$ro = 0$ $ro = 0$

$x = 0$ $x = 1$

$ri = 0$ $ri = 0$

$li = 0$ $li = 0$



CHP: $*[lo\uparrow; [li]; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; ro\downarrow; [\bar{ri}]]$

$x\uparrow$ $x\downarrow$

$lo = 0$ $lo = 0$

$ro = 0$ $ro = 0$

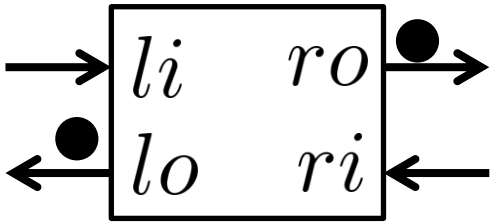
$x = 0$ $x = 1$

$ri = 0$ $ri = 0$

$li = 0$ $li = 0$

PR: $\bar{x} \wedge \bar{lo} \wedge \bar{ro} \wedge \bar{ri} \wedge \bar{li} \rightarrow lo\uparrow$

For lo…

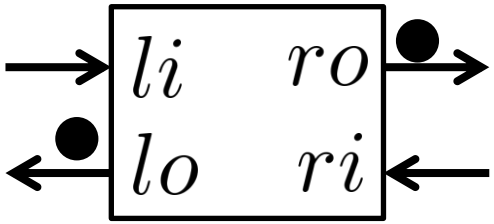


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

PR: $\bar{x} \wedge \bar{lo} \wedge \bar{ro} \wedge \bar{ri} \wedge \bar{li} \rightarrow lo\uparrow$

$\bar{x} \wedge \bar{ri} \rightarrow lo\uparrow$

For lo…



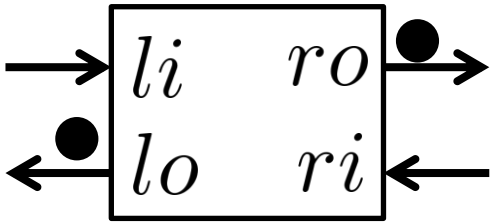
CHP: $*[lo\uparrow; [li]; x\uparrow, lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

PR: $\bar{x} \wedge \bar{lo} \wedge \bar{ro} \wedge \bar{ri} \wedge \bar{li} \rightarrow lo\uparrow$

$\bar{x} \wedge \bar{ri} \rightarrow lo\uparrow$

$x \vee ri \rightarrow lo\downarrow$

For lo…

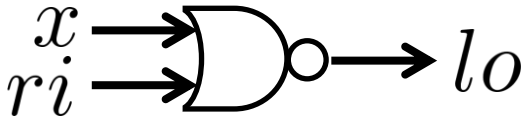


CHP: $*[lo\uparrow; [li]; x\uparrow, lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

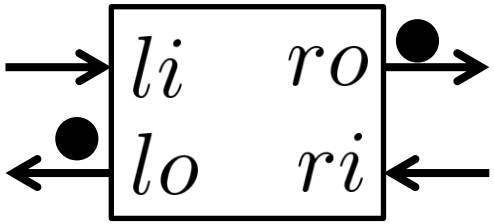
PR: $\bar{x} \wedge \bar{lo} \wedge \bar{ro} \wedge \bar{ri} \wedge \bar{li} \rightarrow lo\uparrow$

$\bar{x} \wedge \bar{ri} \rightarrow lo\uparrow$

$x \vee ri \rightarrow lo\downarrow$



For ro...

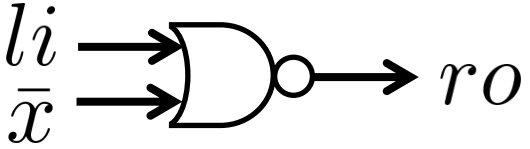


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

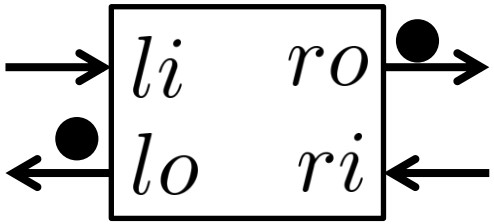
PR:

$$x \wedge \bar{li} \rightarrow ro\uparrow$$

$$\bar{x} \vee li \rightarrow ro\downarrow$$

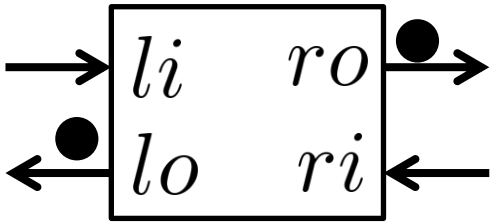


For x...



CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

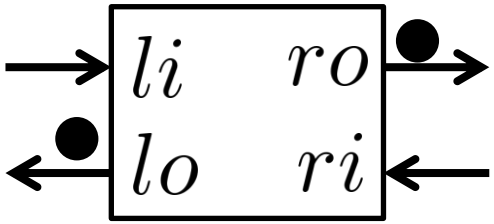
For x…



CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

… What gate is this?

For x...

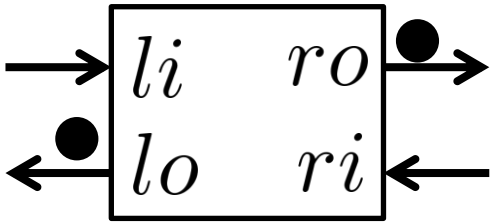


CHP: $*[lo\uparrow;[li];x\uparrow;lo\downarrow;[\bar{li}];ro\uparrow;[ri];x\downarrow;ro\downarrow;[\bar{ri}]]$

PR: $\bar{ri} \wedge li \rightarrow x\uparrow$

$ri \wedge \bar{li} \rightarrow x\downarrow$

For x...

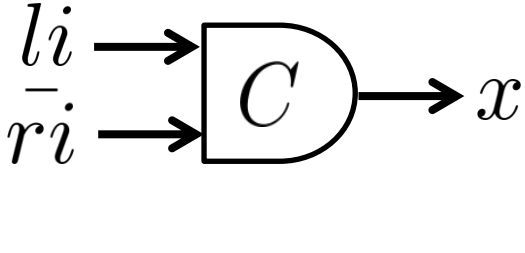


CHP: $*[lo\uparrow;[li];x\uparrow;lo\downarrow;[\bar{li}];ro\uparrow;[ri];x\downarrow;ro\downarrow;[\bar{ri}]]$

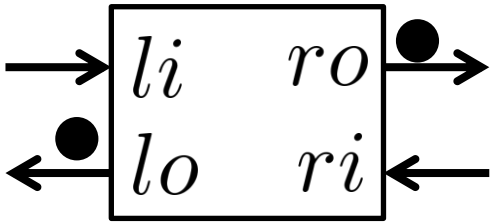
PR:

$$\bar{ri} \wedge li \rightarrow x\uparrow$$

$$ri \wedge \bar{li} \rightarrow x\downarrow$$

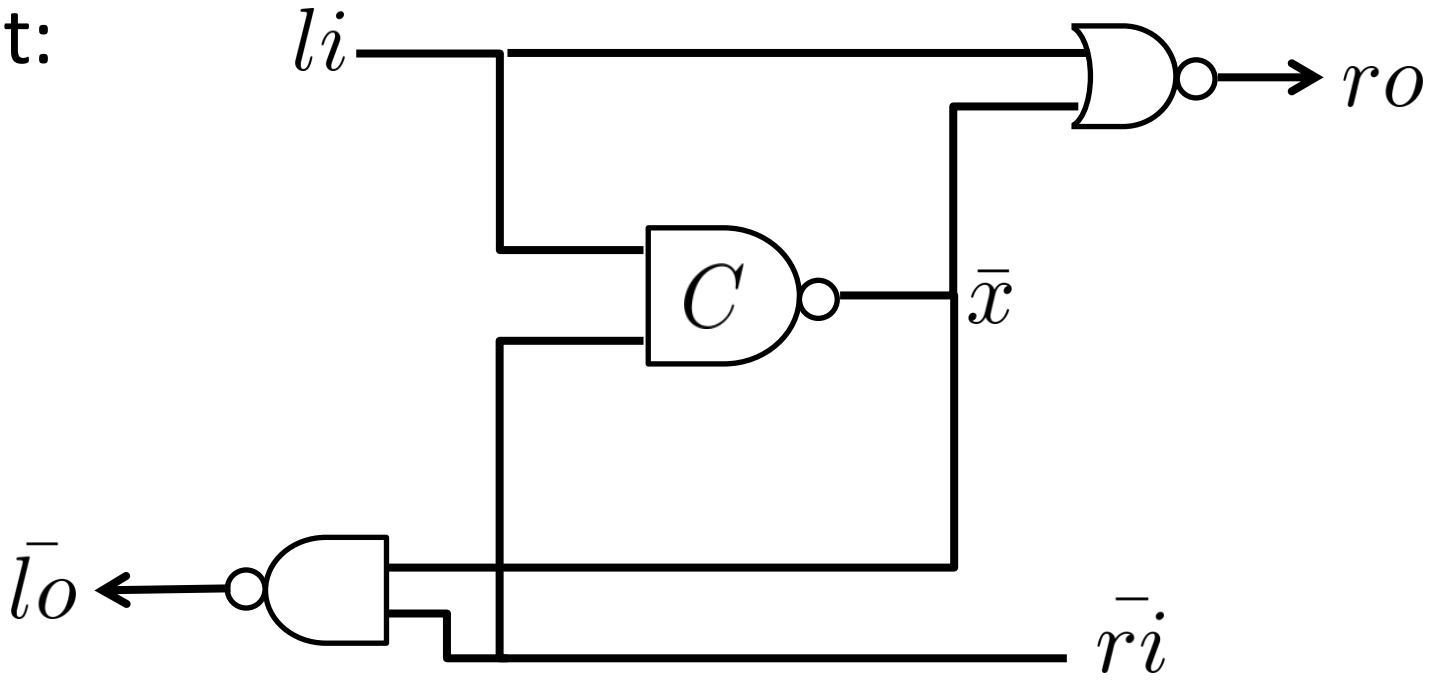


Putting it together

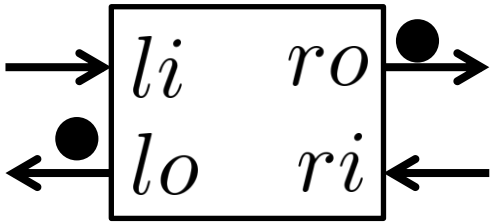


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:

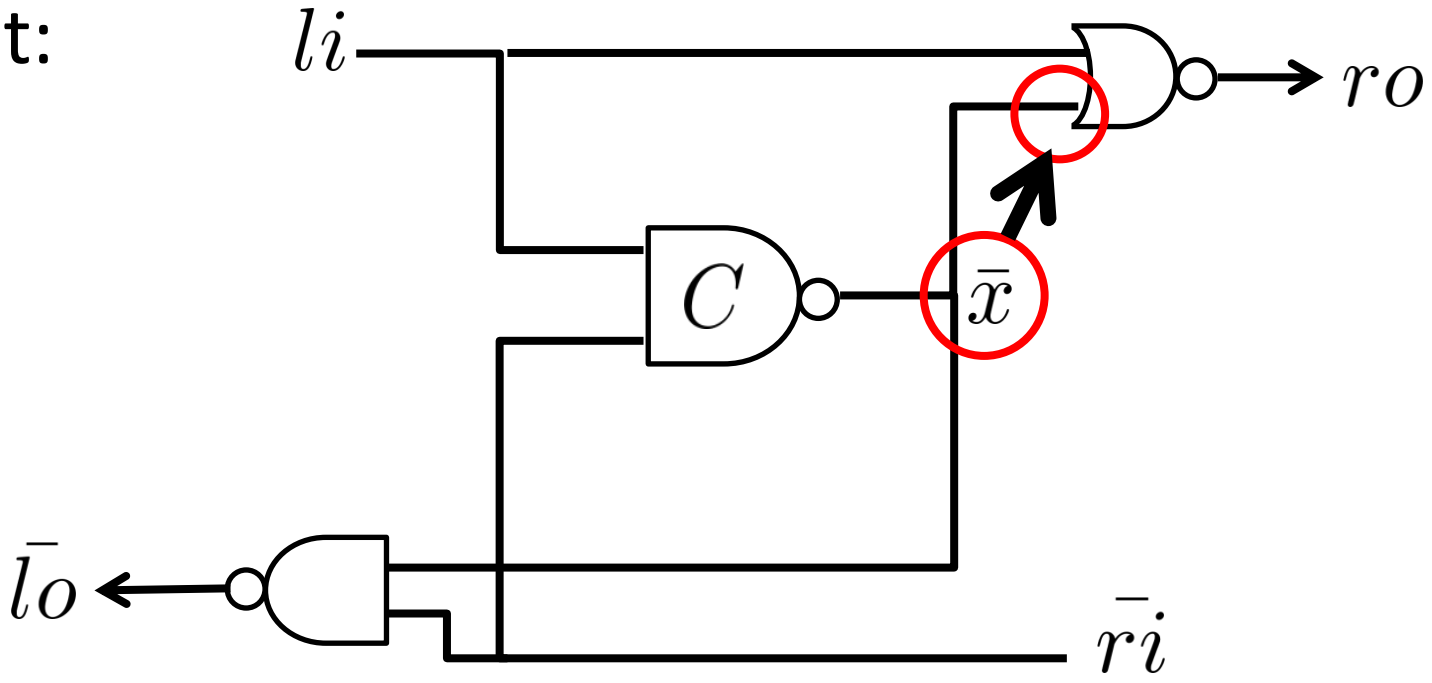


Mind wires...

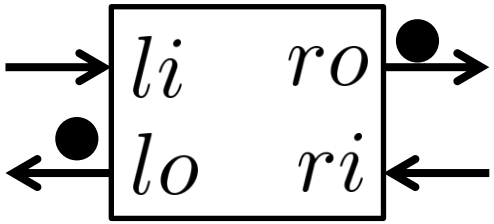


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:

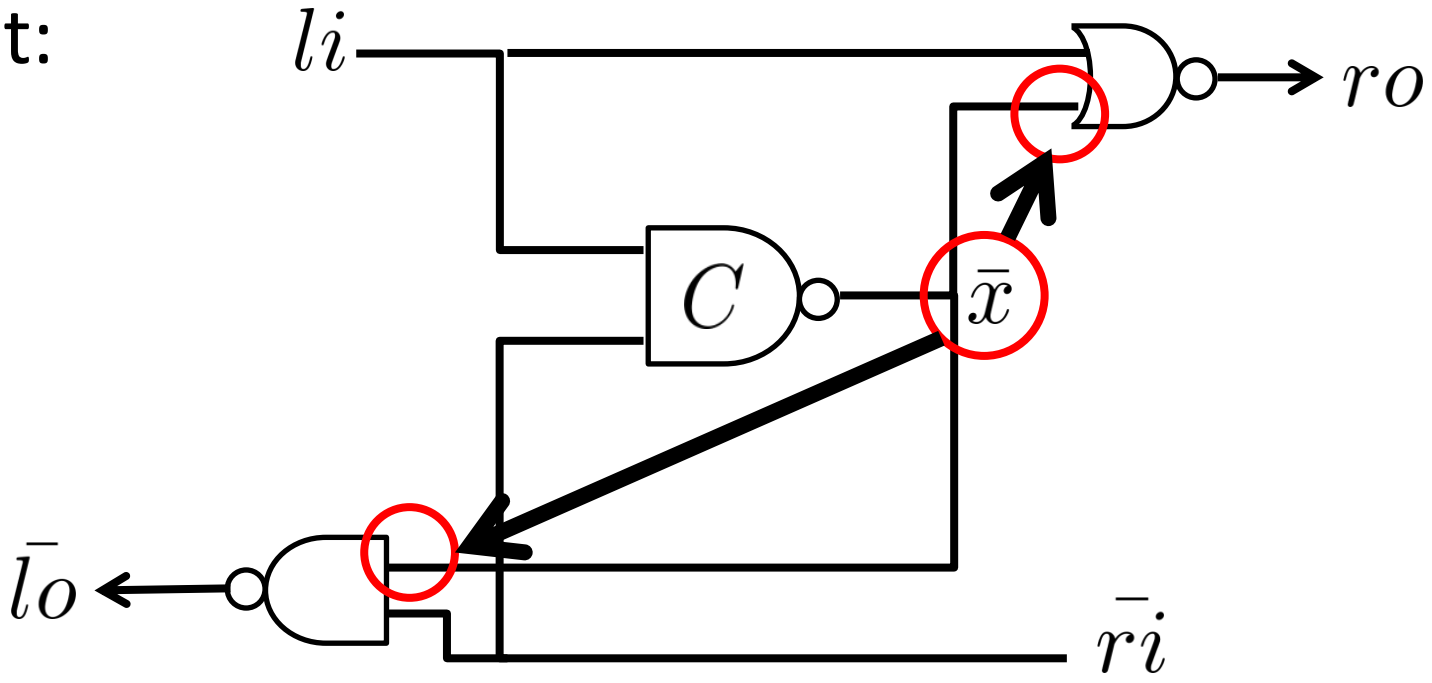


Mind forks...

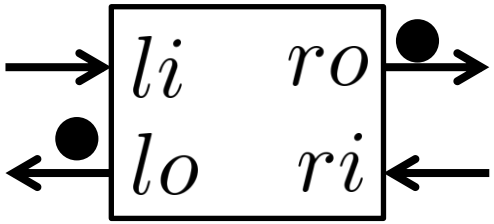


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:

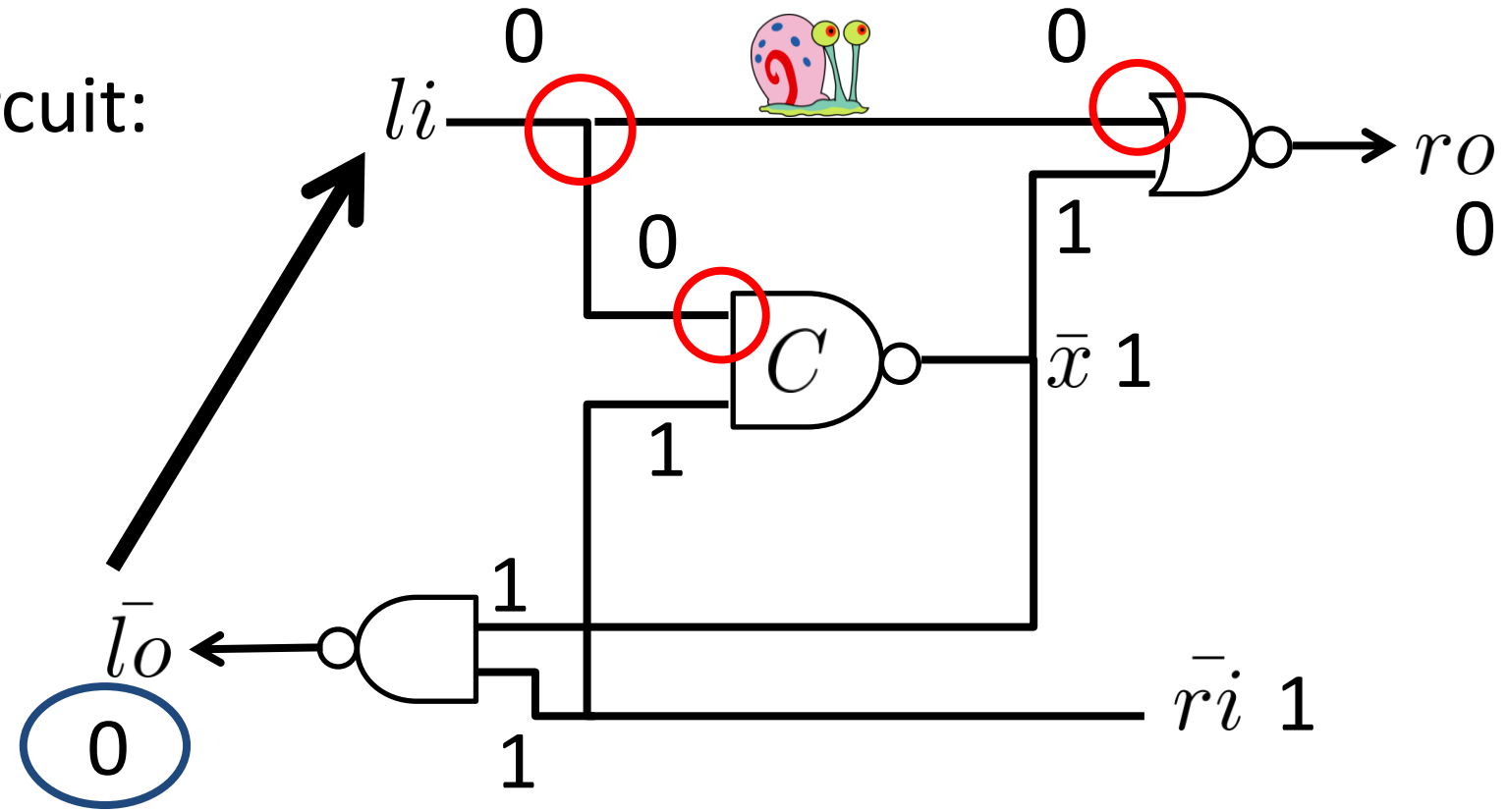


Checking fork "li" (1)

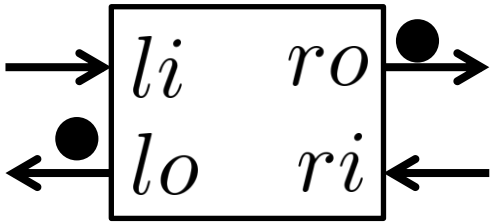


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:

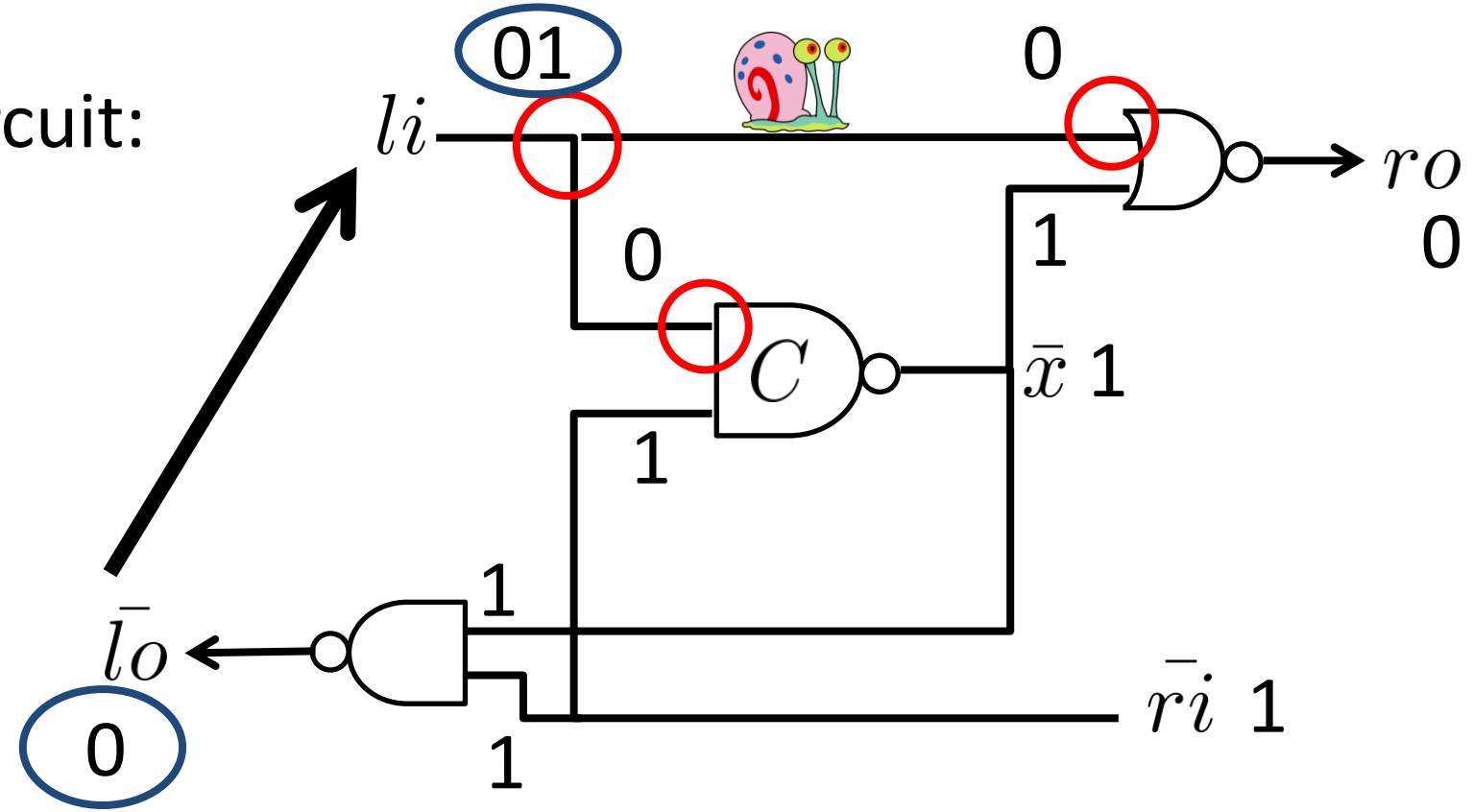


Checking fork "li" (1)

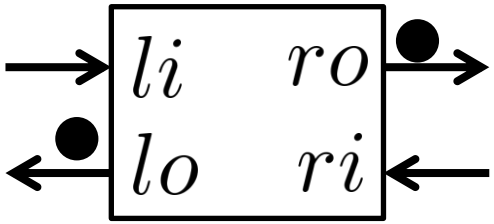


CHP: $*[lo\uparrow [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:

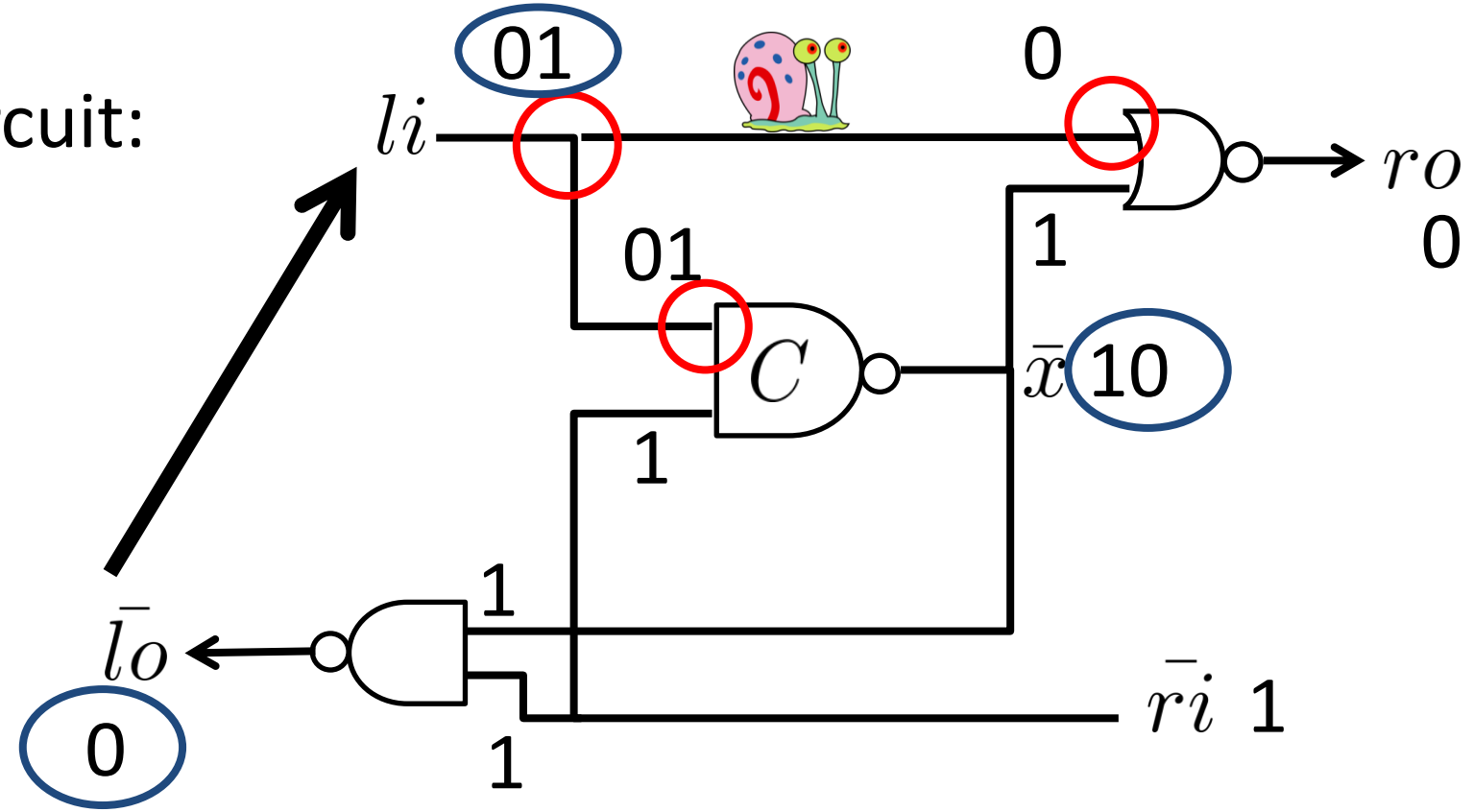


Checking fork "li" (1)

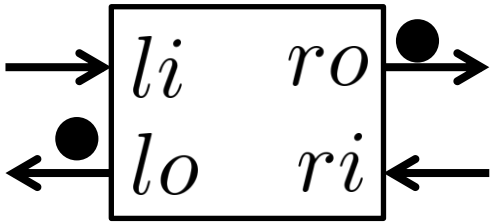


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:

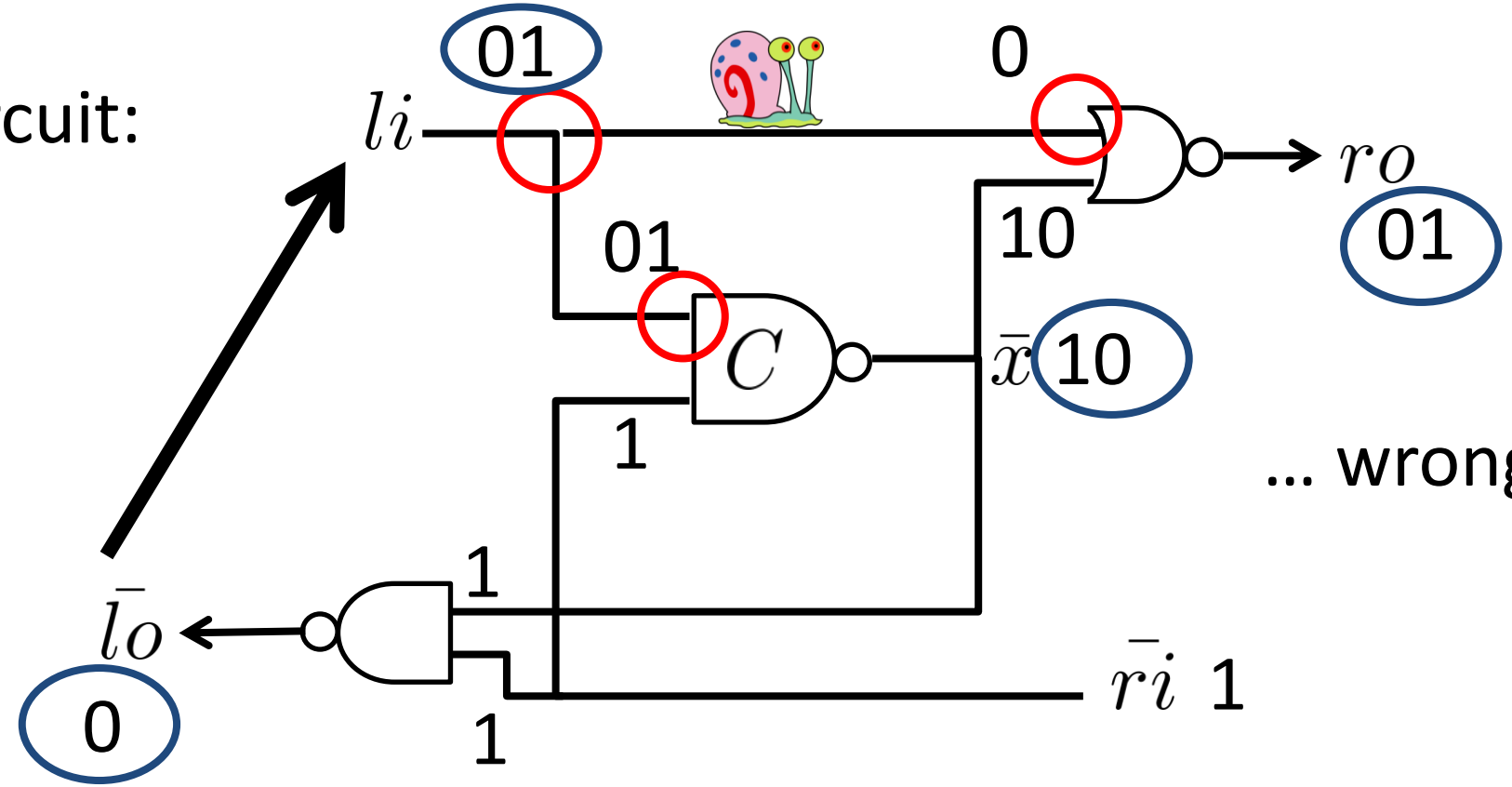


Checking fork "li" (1)

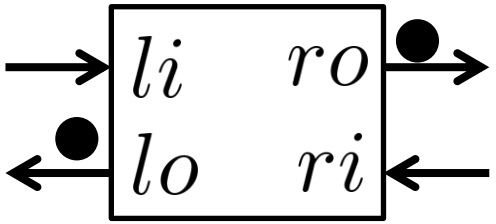


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:

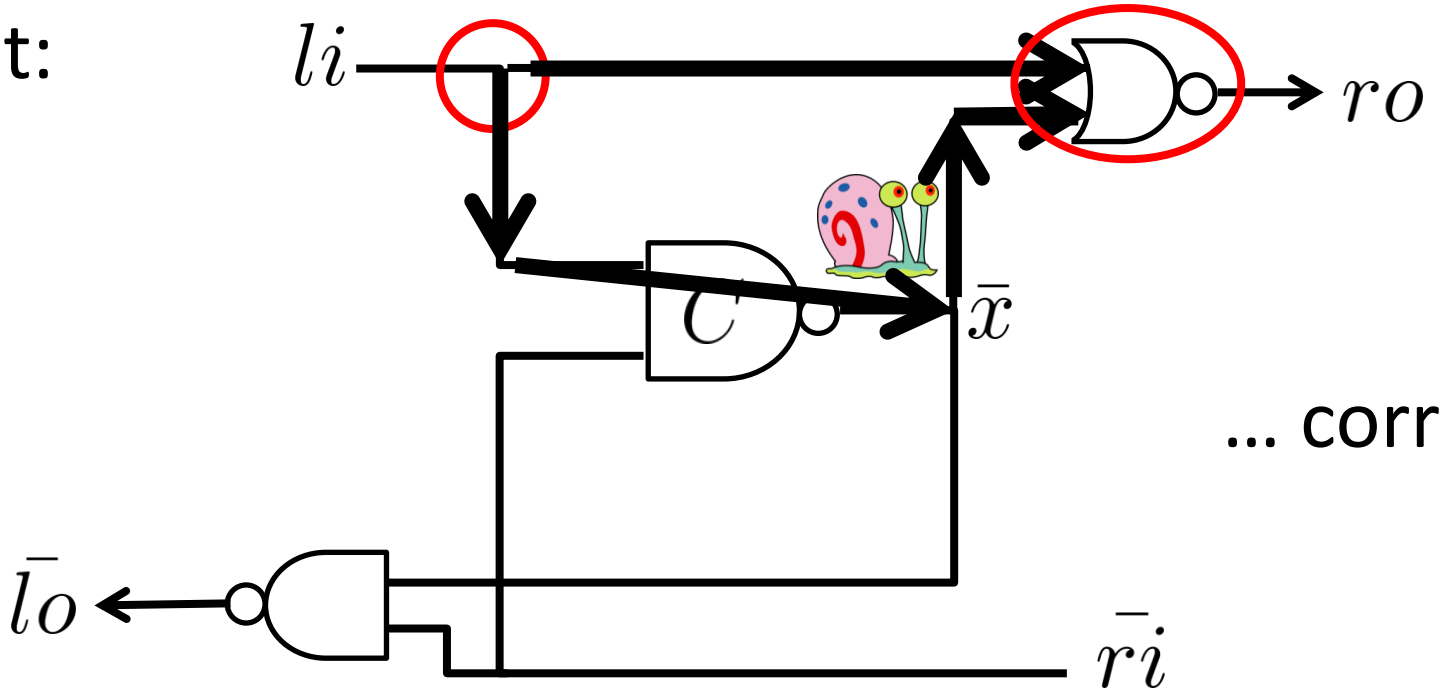


+ one-sided Constraint



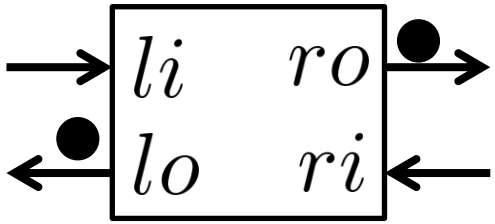
CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Circuit:



… correct.

+ one-sided Constraint



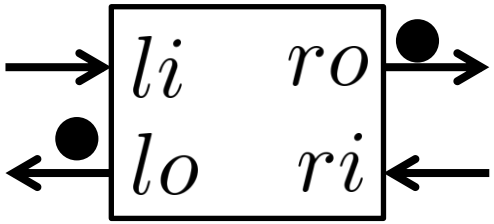
CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

Proving correct:

e.g. by induction.

base case: start with initial states and prove ordering of events from there for the first loop

+ one-sided Constraint



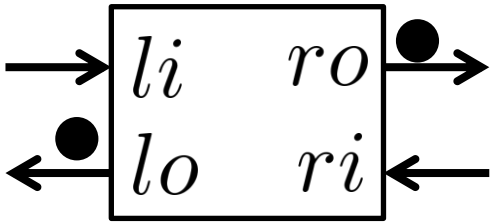
CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

proof:

examine ordering in time "<".

1) **lo-up < [li]:** guaranteed by environment: Initially li = 0. Can be set to li = 1 only by environment. Environment does this only after lo = 1.

+ one-sided Constraint

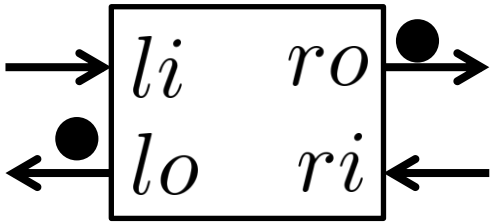


CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

proof:

2) **[li] < x-up:** x = 1 can happen only after both C-Element inputs are 1. This can happen only after li = 1 for the first time.

+ one-sided Constraint



CHP: $*[lo\uparrow; [li]; x\uparrow; lo\downarrow; [\bar{li}]; ro\uparrow; [ri]; x\downarrow; ro\downarrow; [\bar{ri}]]$

proof:

3) **x-up < lo-down:** this can happen only if one of the NAND inputs becomes 0 for the first time.

We first show that lo-down cannot happen because of the input connected to not ri becoming 0: .....

[hw project]

Hw project

- Prove: PR circuit implements CHP circuit:

  all executions generated by PR circuit fulfil CHP properties.

- Use: NuSMV

  model checker

  see e.g. nusmv.fbk.eu/NuSMV/tutorial

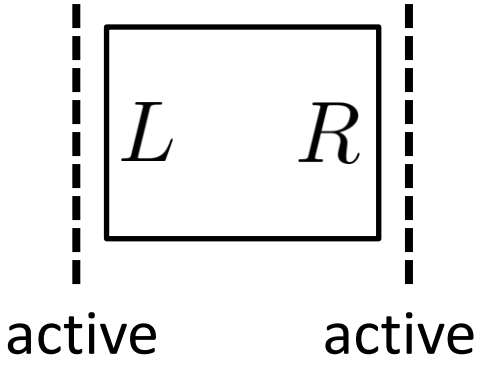
Hw project

- Input:
  - automaton specification (PRs) + fairness condition
  - Linear Temporal Logic (LTL) formula to verify
- Output:
  - formula holds vs. does not hold + counterexample

active -> passive

active L, active R,

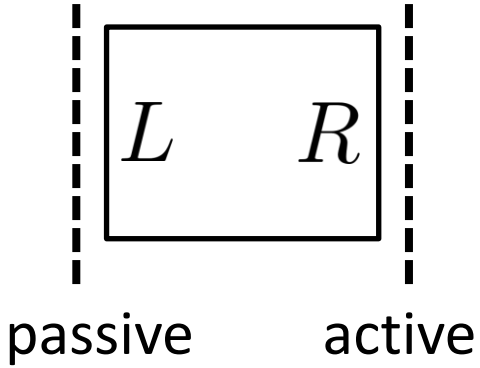
CHP: $P1 : *[L; R]$



→

passive L, active R,

CHP:

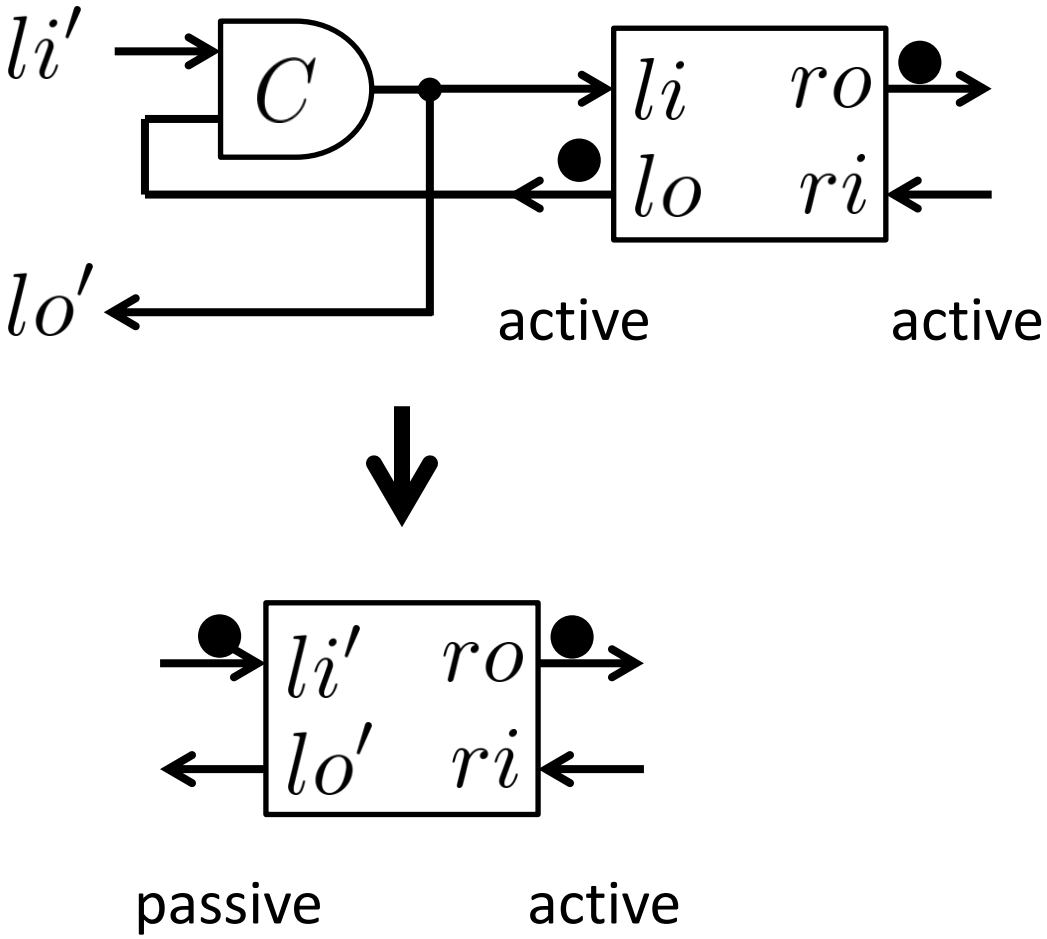


4ph-hs active -> passive

active active

passive active

4ph-hs active -> passive



[hw]

Beyond classical circuit design lecture 6.5

Gate internals

Further Reading

Simon M. Sze, Kwok K. Ng: *Physics of Semiconductor Devices. 3rd edition.* Wiley, 2006.

Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic: *Digital Integrated Circuits. A Design Perspective. 2nd edition.* Prentice Hall, 2003.

Why look inside?

- Why is stability important?

  -> Runts/metastability

- What if it does not hold?

  -> Dealing with them.

- Optimization for speed/power/size/robustness...

In principle…

Schrödinger equation in space and time

$$i\hbar\frac{\partial}{\partial t}\psi(x,t) = H\psi(x,t)$$

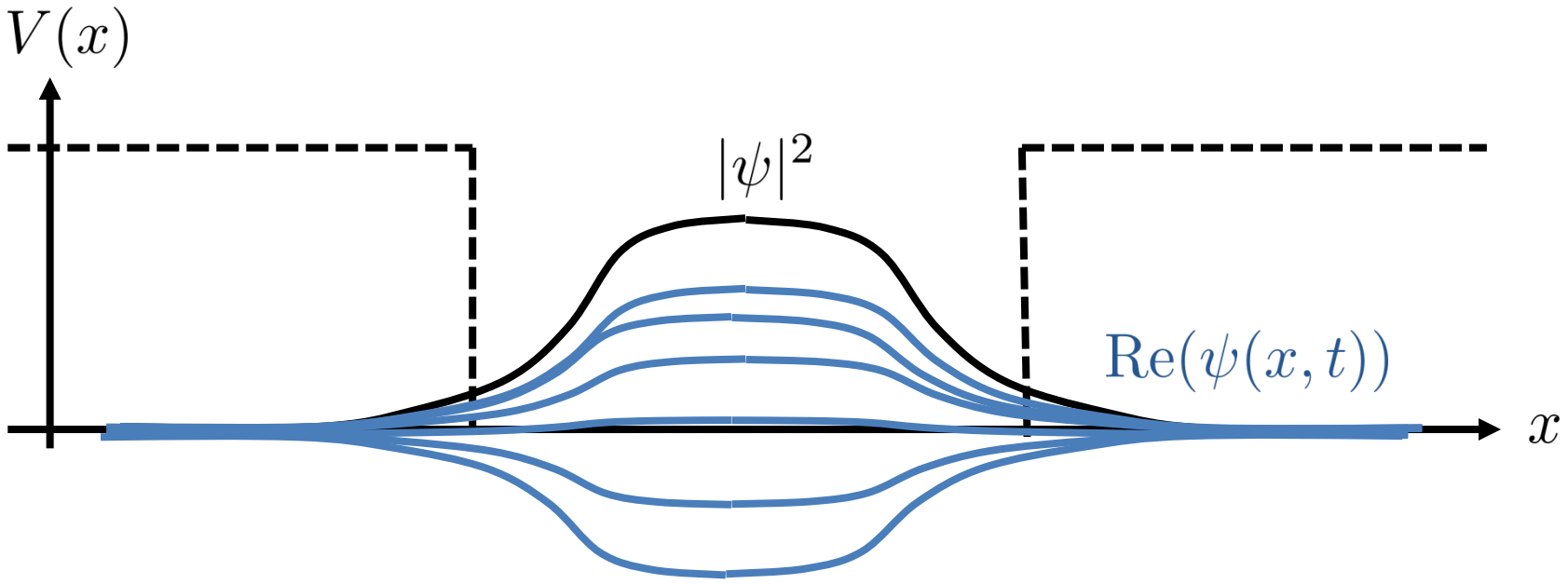
in one dimension

$$i\hbar\frac{\partial}{\partial t}\psi(x,t) = -\frac{\hbar\partial^2}{2m\partial x^2}\psi(x,t) + V(x,t)\psi(x,t)$$

In principle…

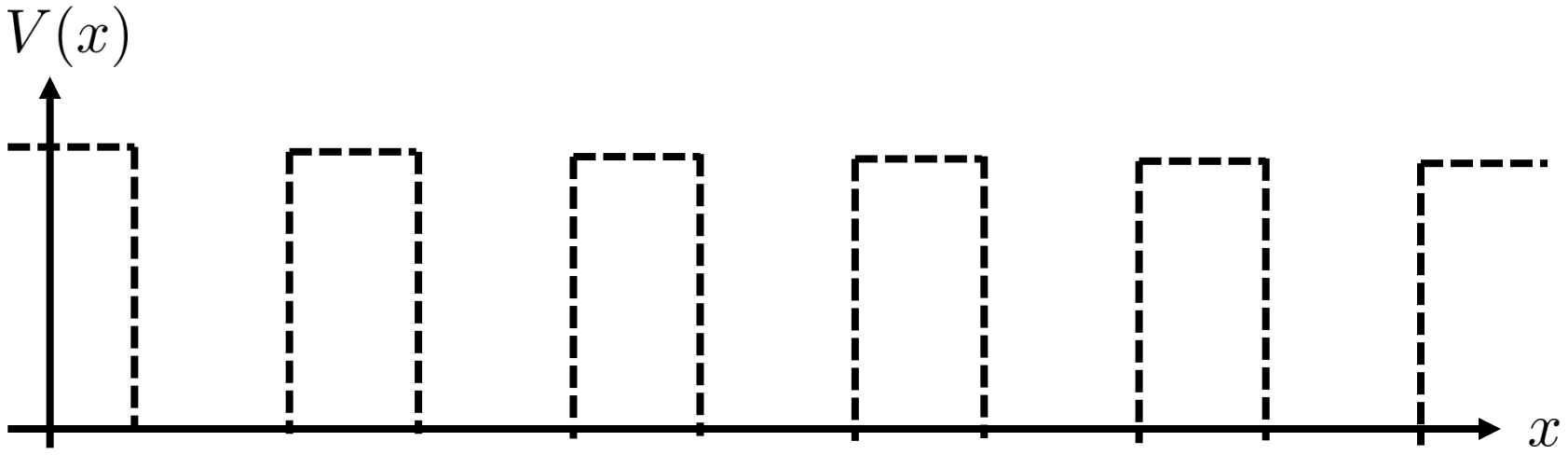
assuming steady state

$$\psi(x,t) = e^{i\omega t}\psi(x)$$



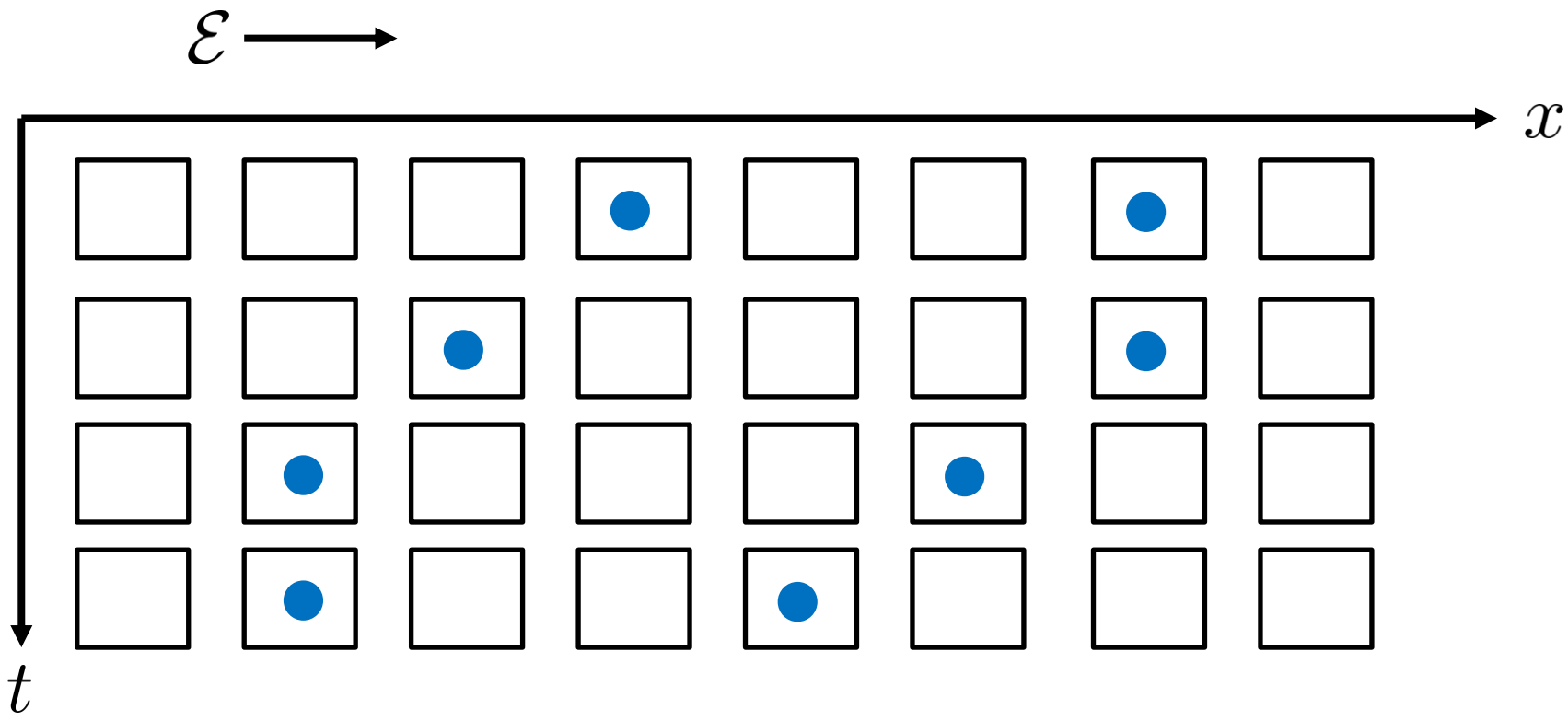
In principle…

simplified model: single e- in periodic potential



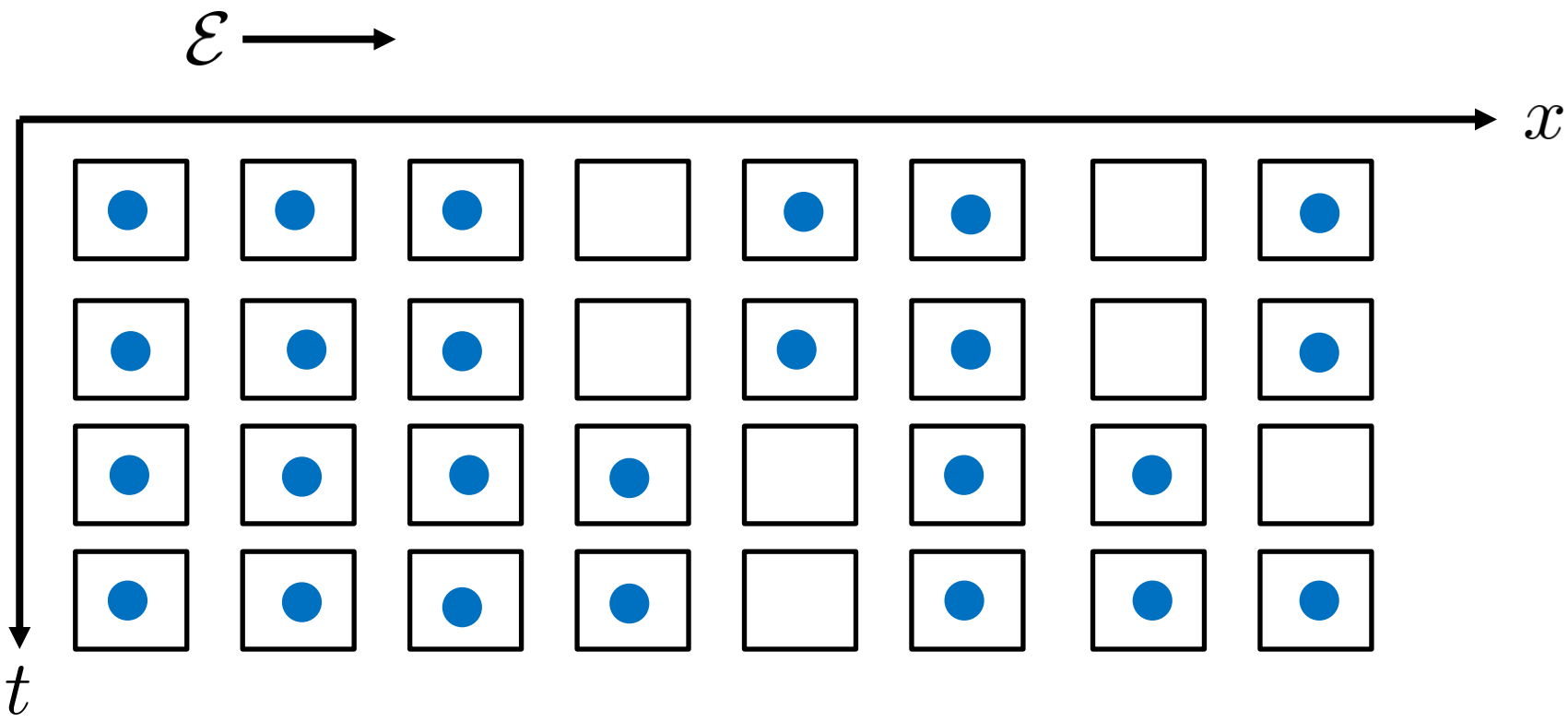
Carriers

e^- electron



Carriers

e^- electron



Carriers

e^- electron h^+ hole