Beyond classical circuit design lecture 7

Gate internals continued

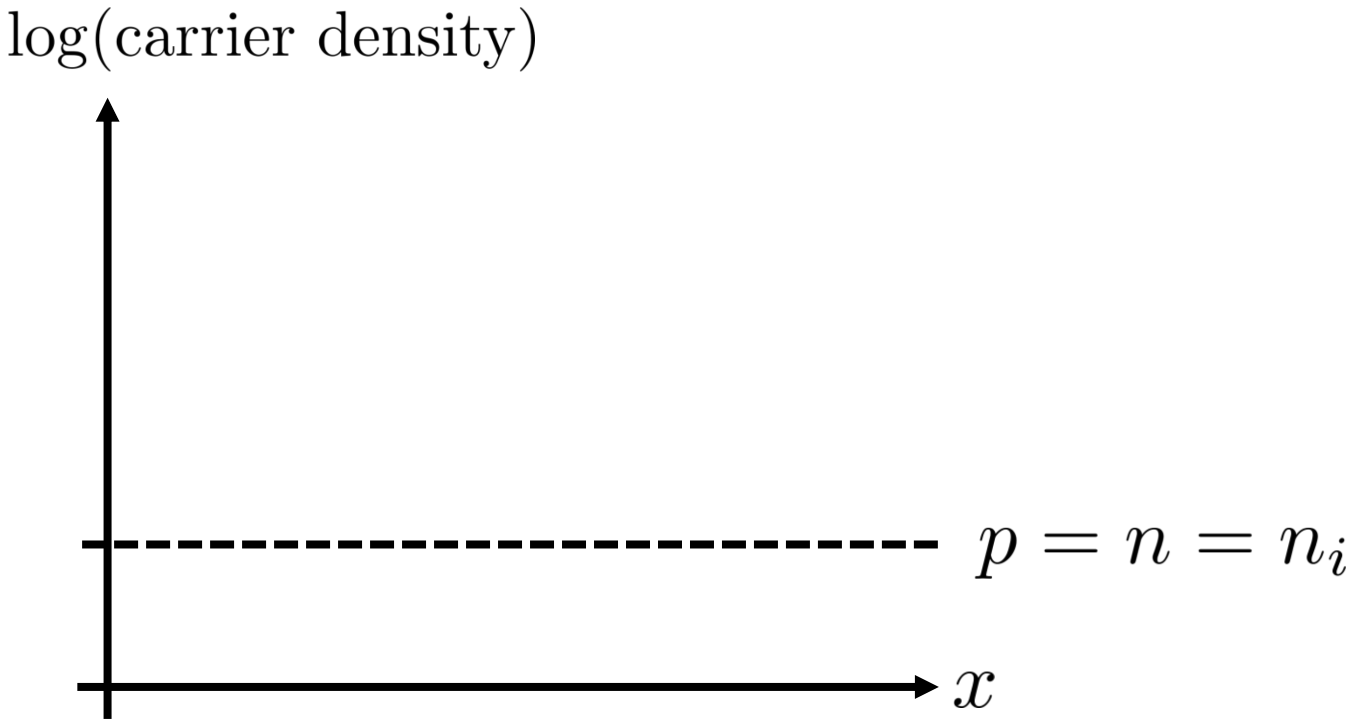
Further Reading

Simon M. Sze, Kwok K. Ng: *Physics of Semiconductor Devices. 3rd edition.* Wiley, 2006.

Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic: *Digital Integrated Circuits. A Design Perspective. 2nd edition.* Prentice Hall, 2003.

Carrier densities

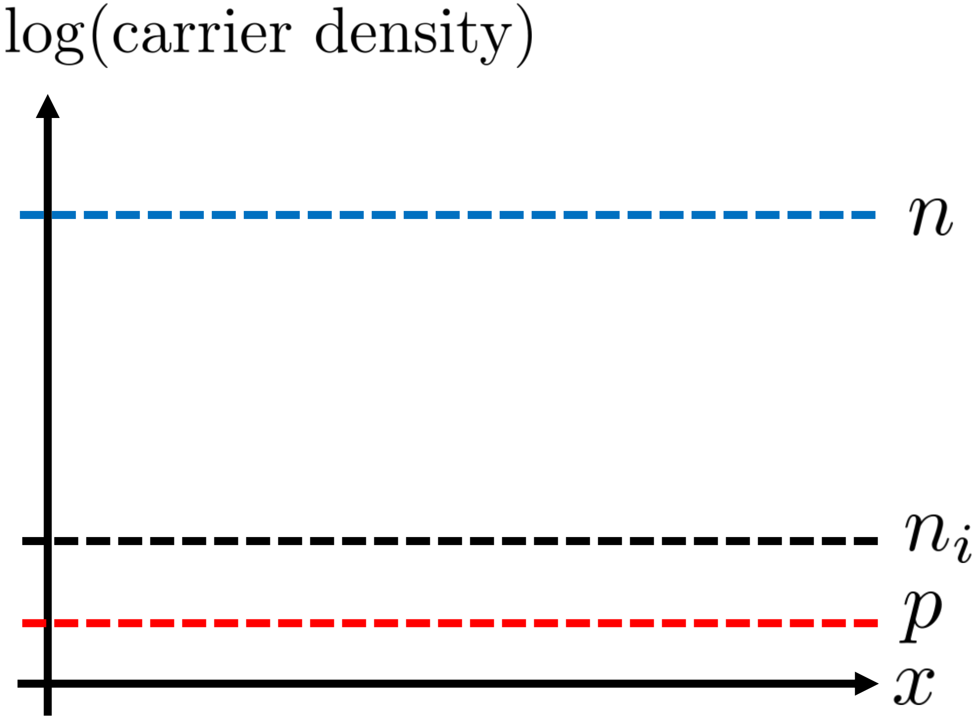
semiconductor at thermal equilibrium



Carrier densities

adding donor atoms -> n-doped semiconductor

-> free e-



mass-action law

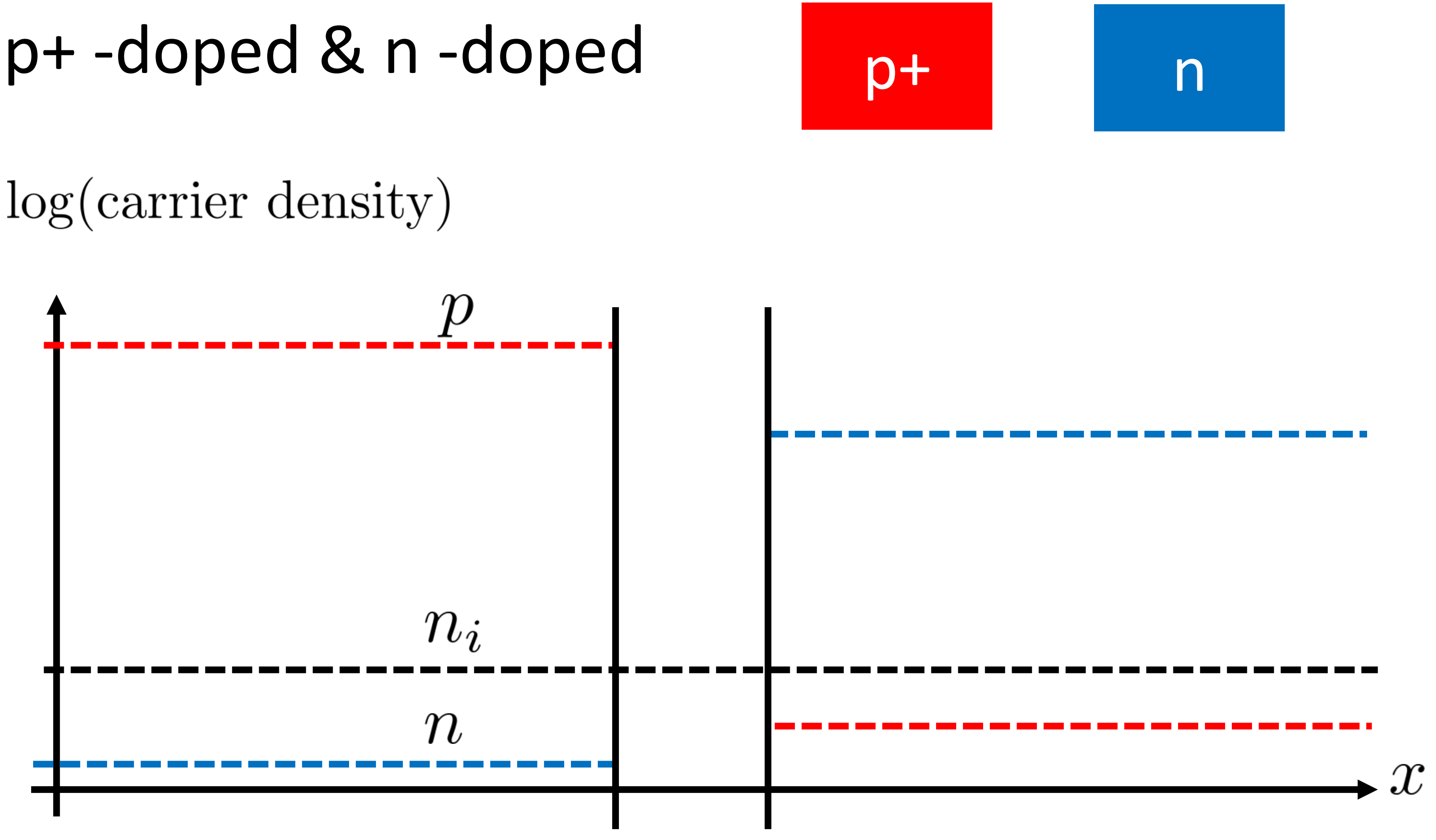
$$pn = n_i^2$$

charge neutrality

$$n + N_A^- = p + N_D^+$$

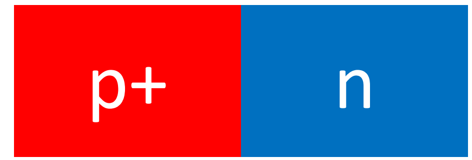
Carrier densities

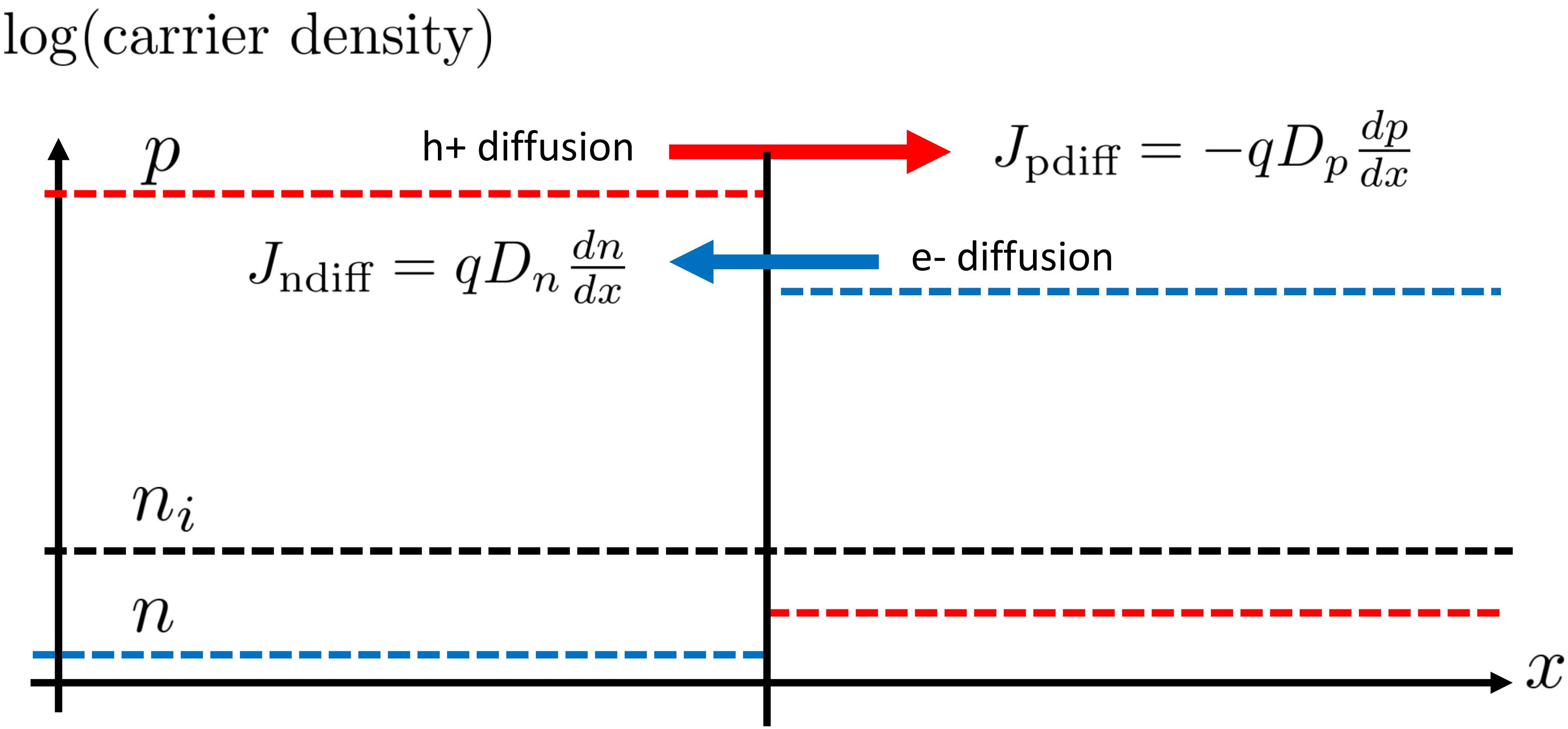
p+ -doped & n -doped



Diffusion

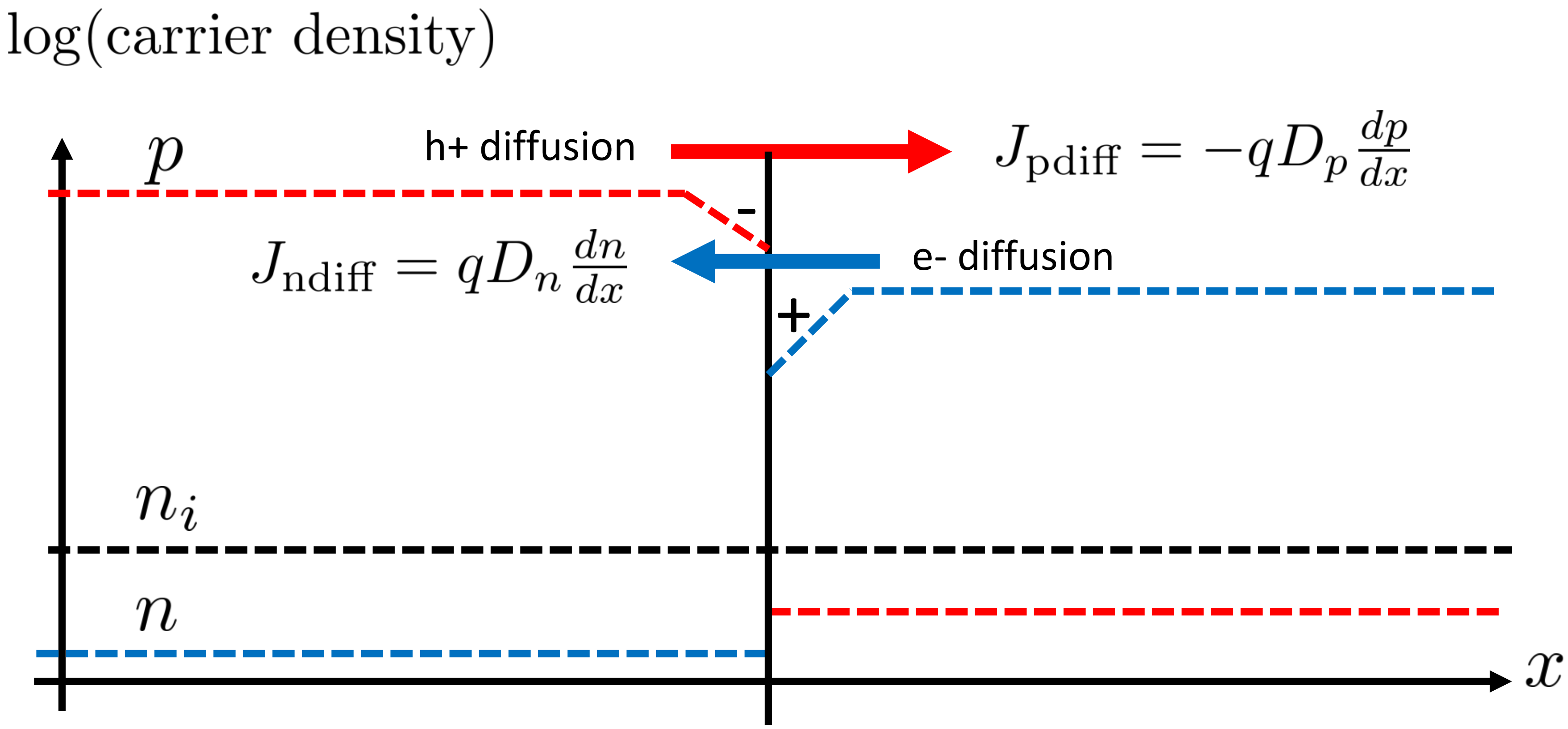
merging p+ -doped & n -doped





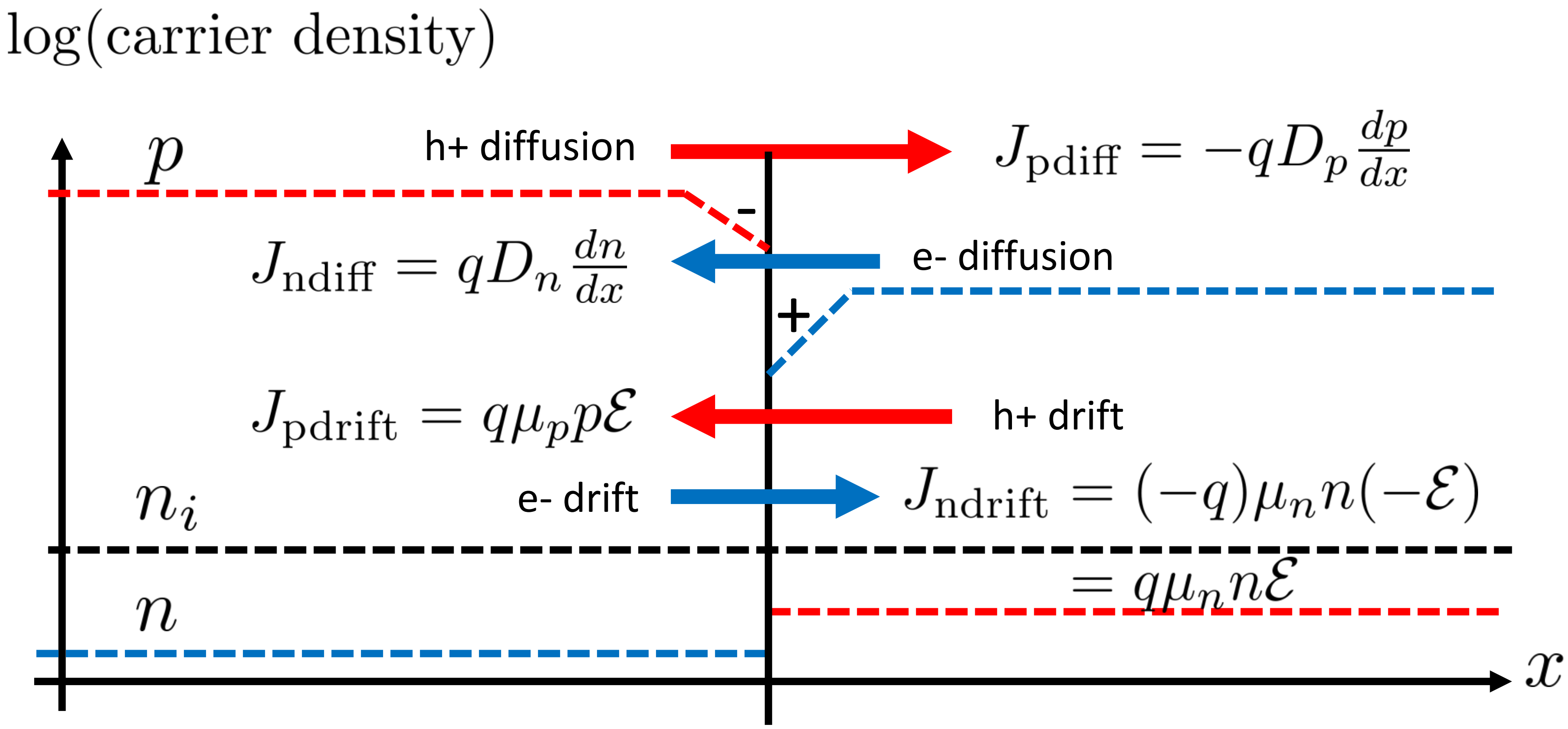
Diffusion

merging p+ -doped & n -doped



Drift

merging p+ -doped & n -doped



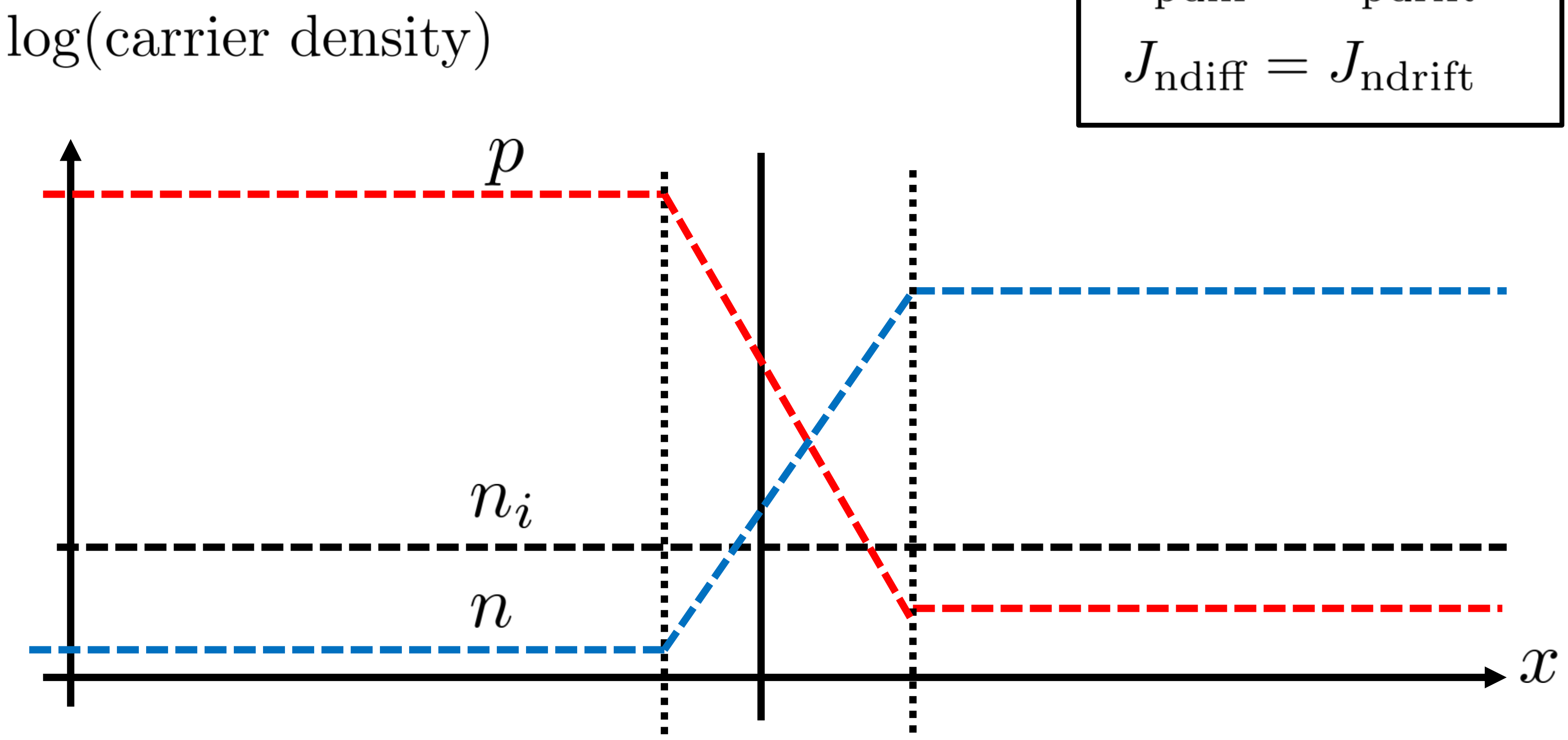
Equilibrium carrier densities

merging p+ -doped & n -doped

equilibrium

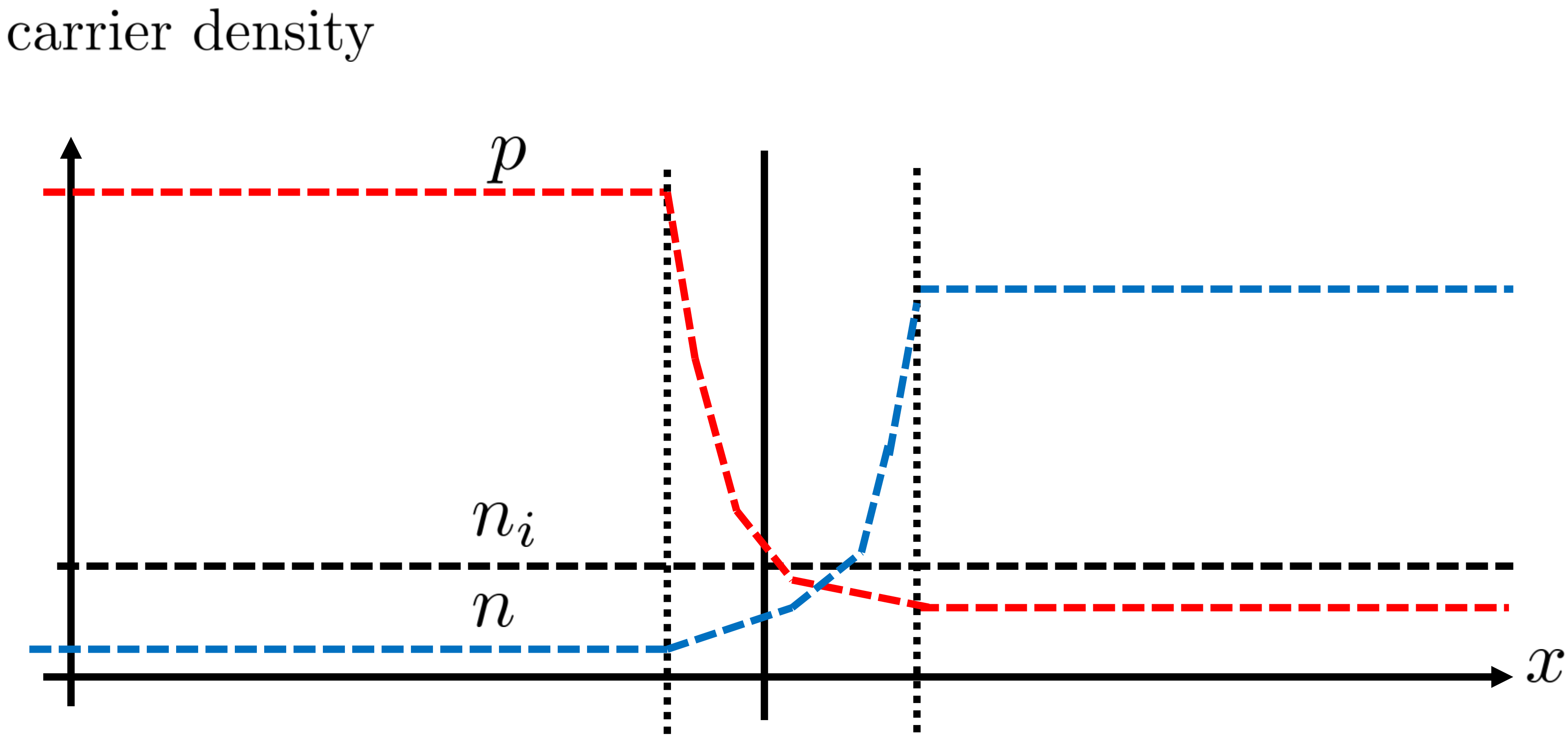
$$J_{\text{pdiff}} = J_{\text{pdrift}}$$

$$J_{\text{ndiff}} = J_{\text{ndrift}}$$



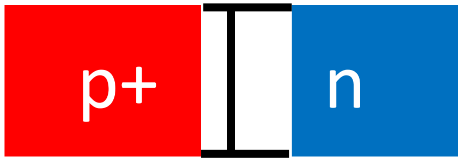
Carrier densities

merging p+ -doped & n -doped

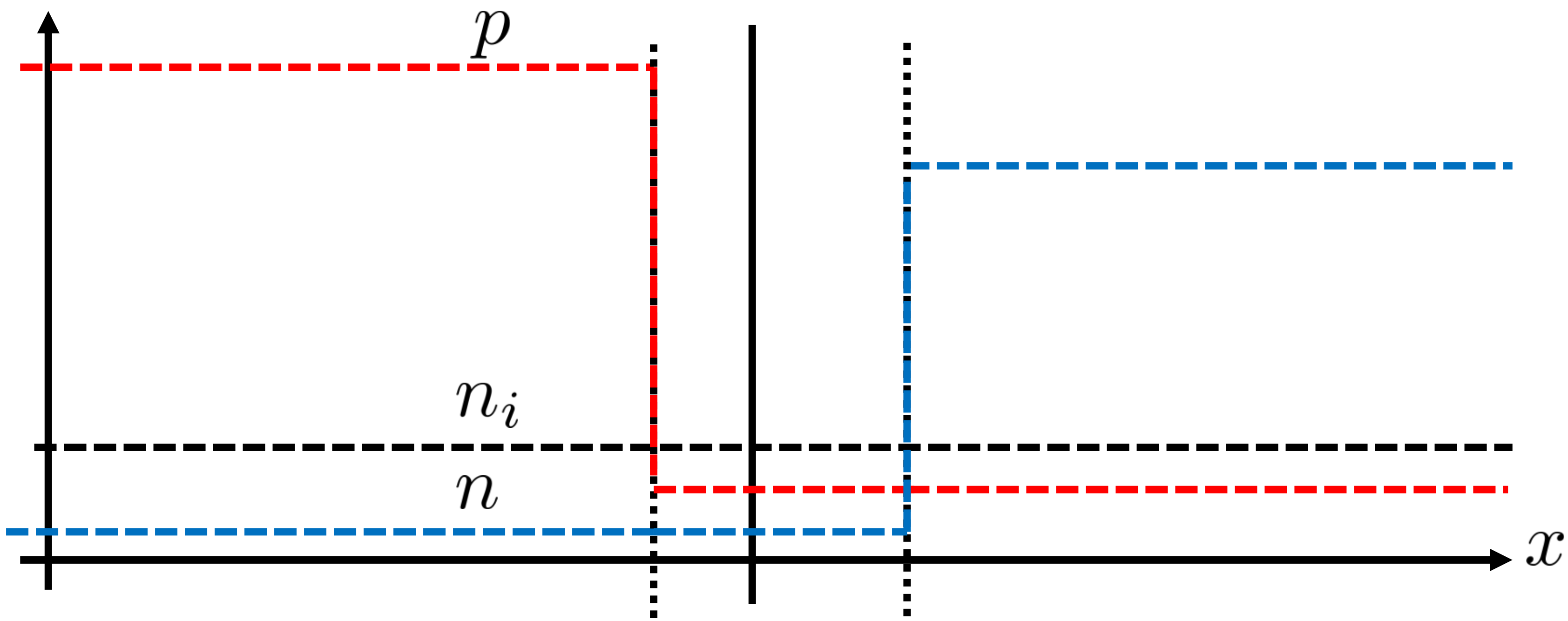


Carrier densities

A1. box profile approximation



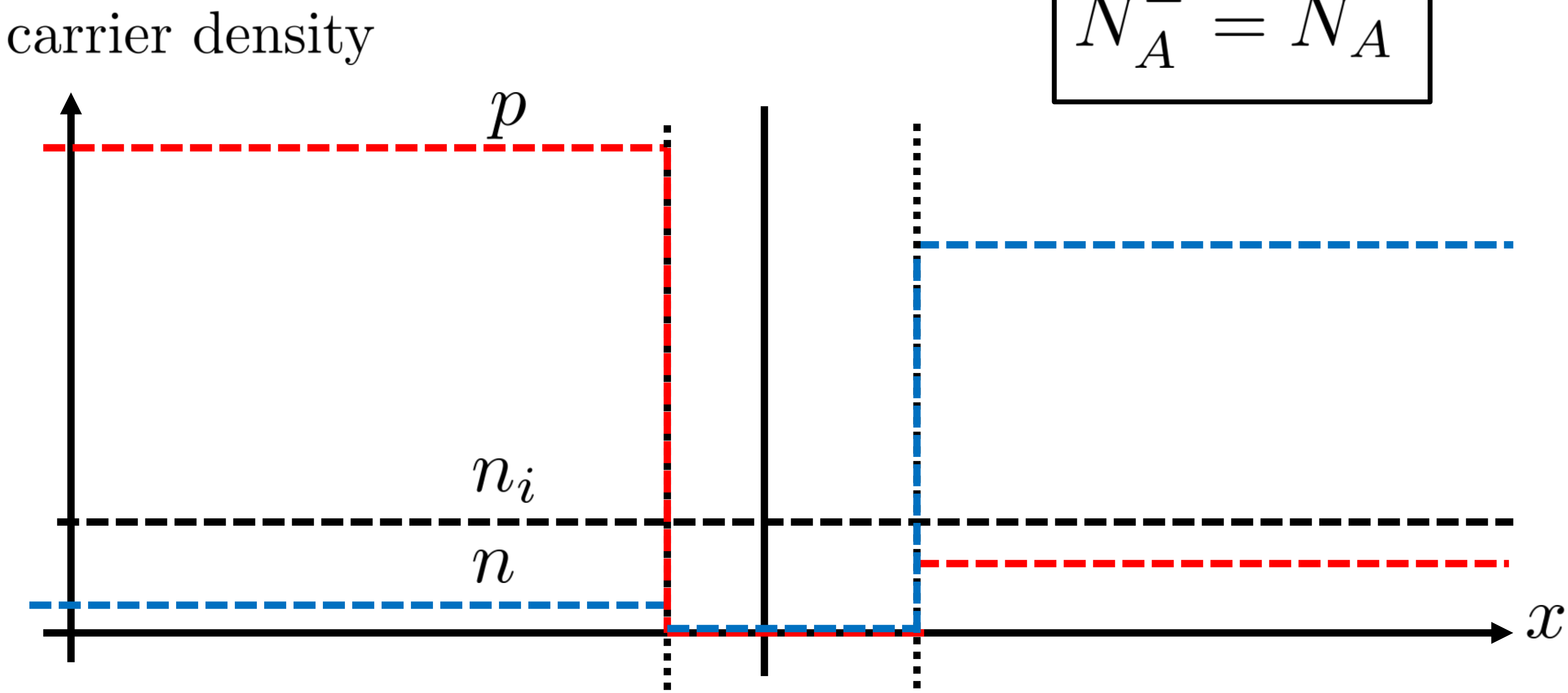
carrier density



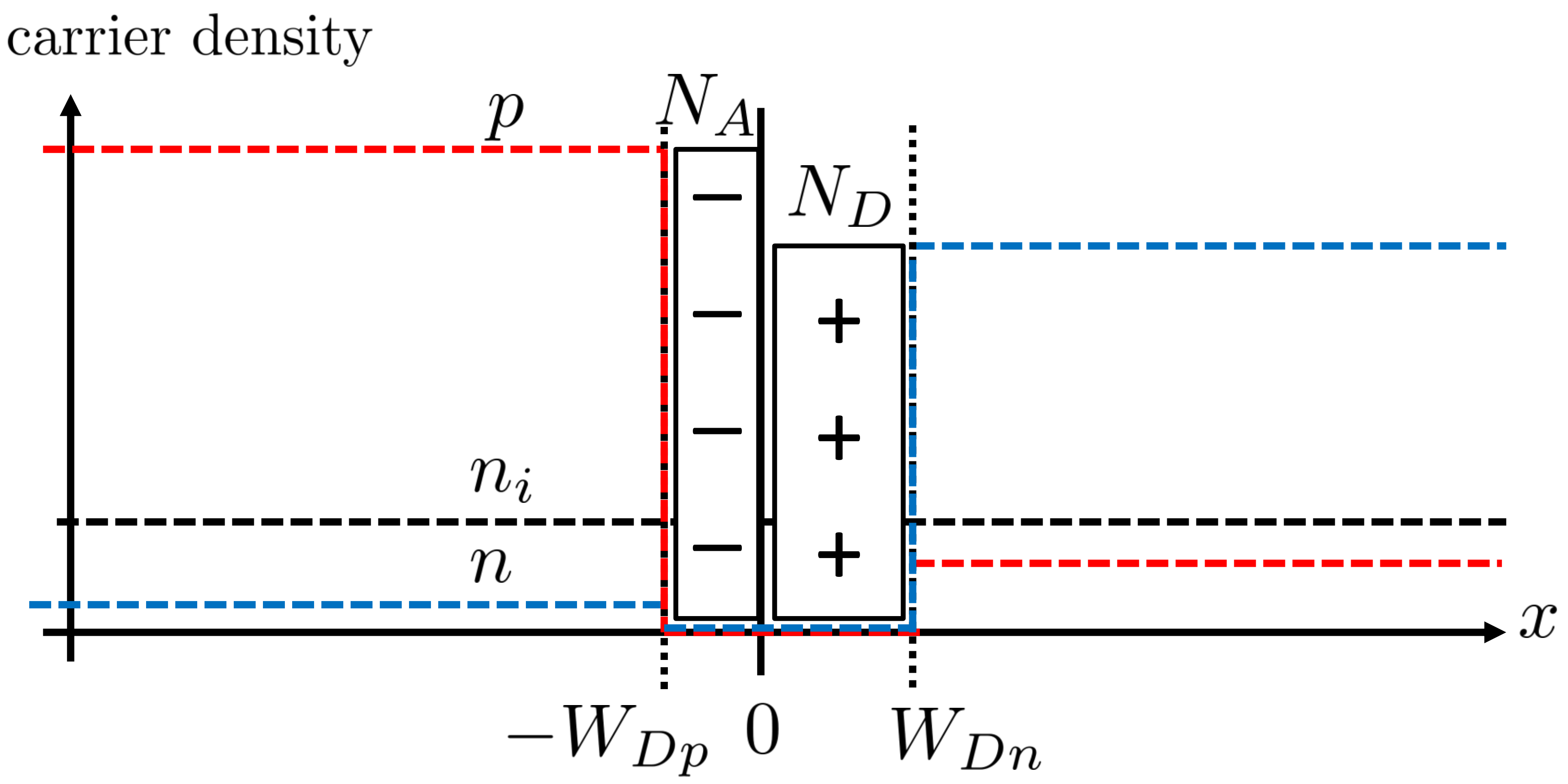
Carrier densities

A2. depletion region: no free carriers $n = p = 0$

A3. all donors/acceptors ionized $N_D^+ = N_D$ $N_A^- = N_A$

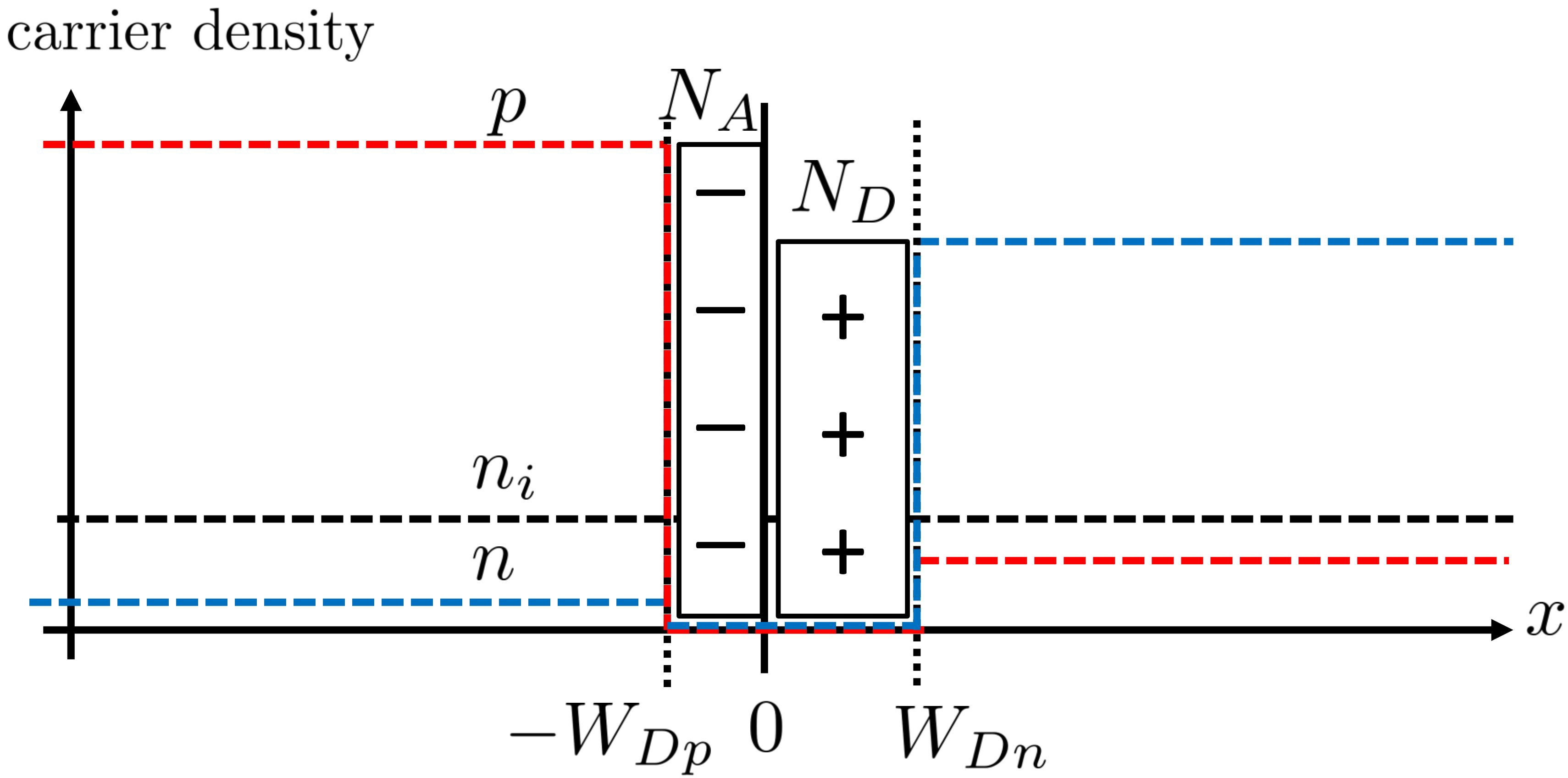


Carrier densities

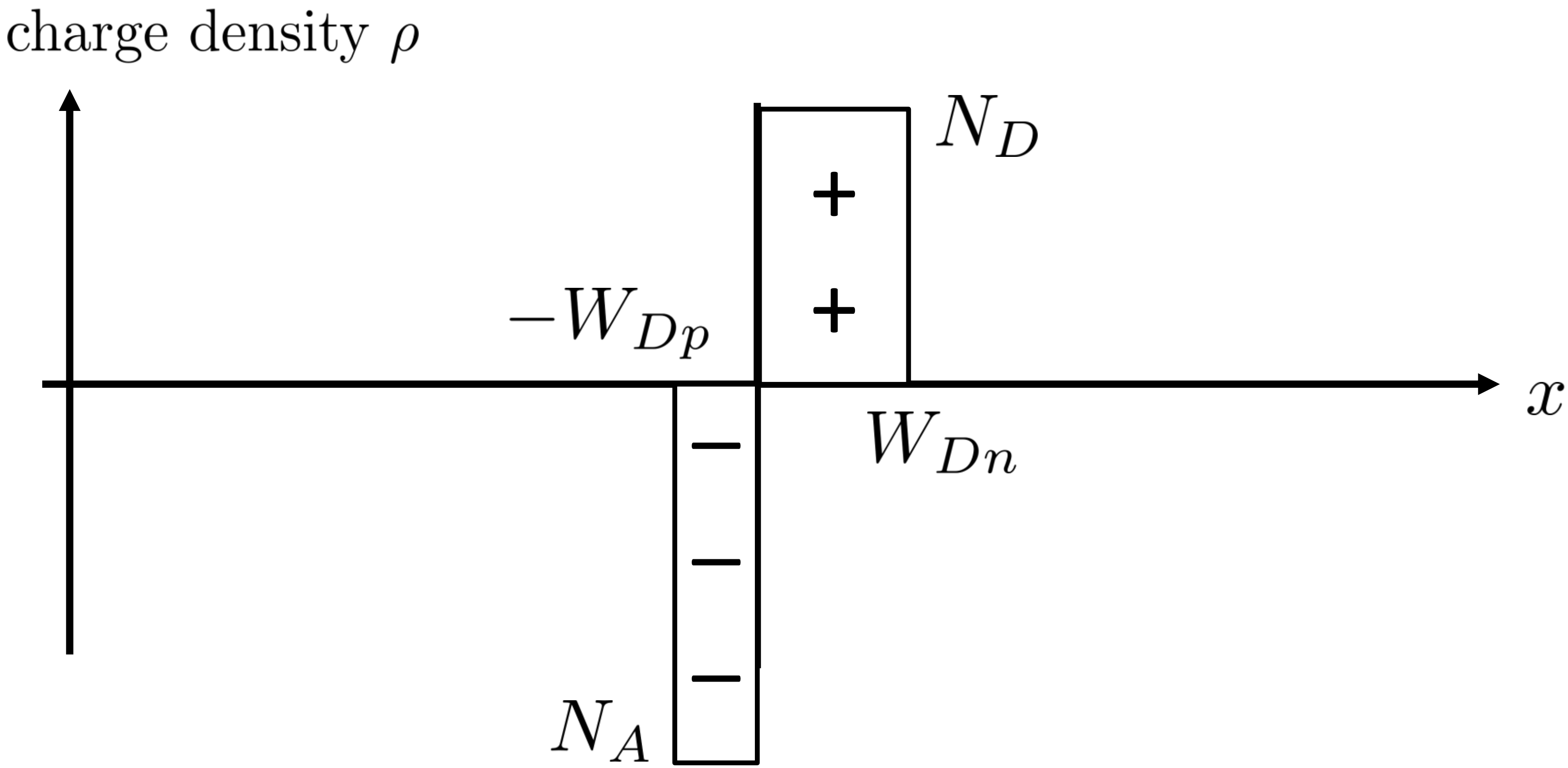


Carrier densities

neutrality $N_D W_{Dn} = N_A W_{Dp}$

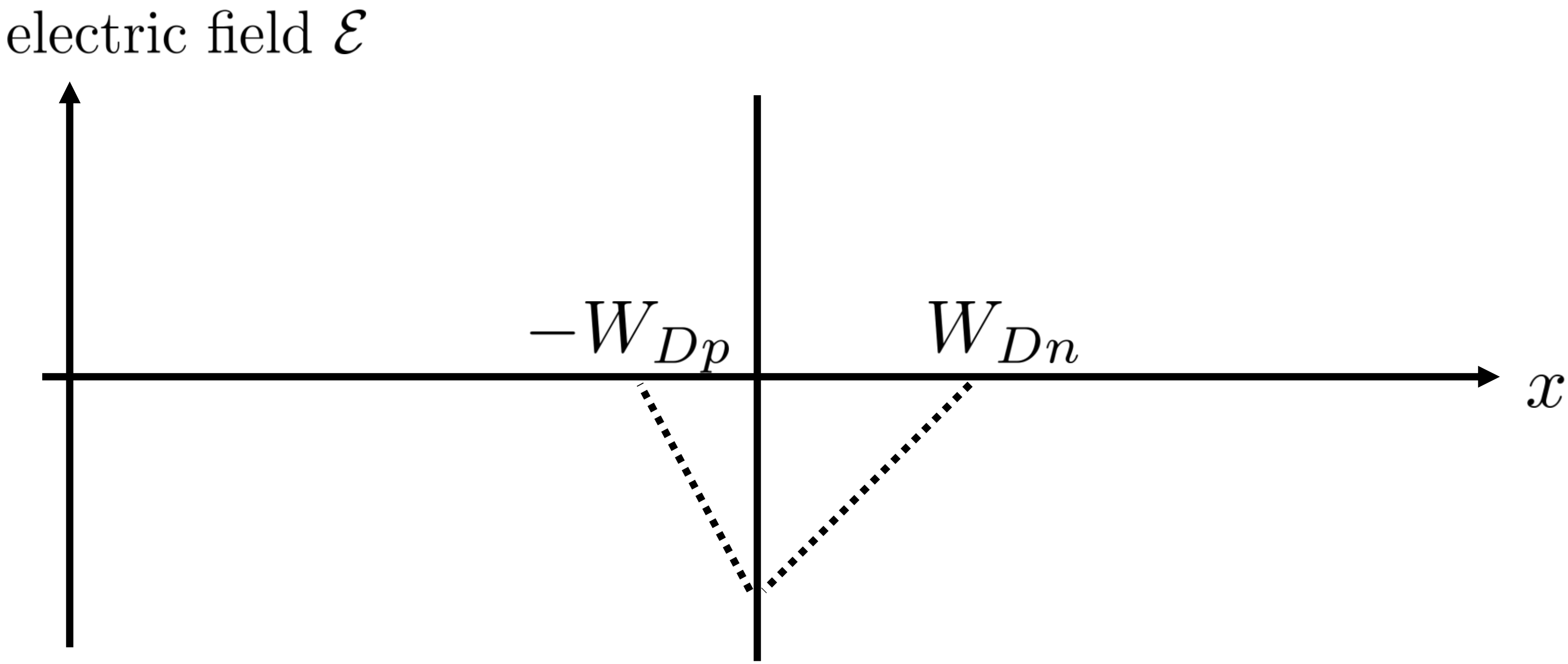


Charge density



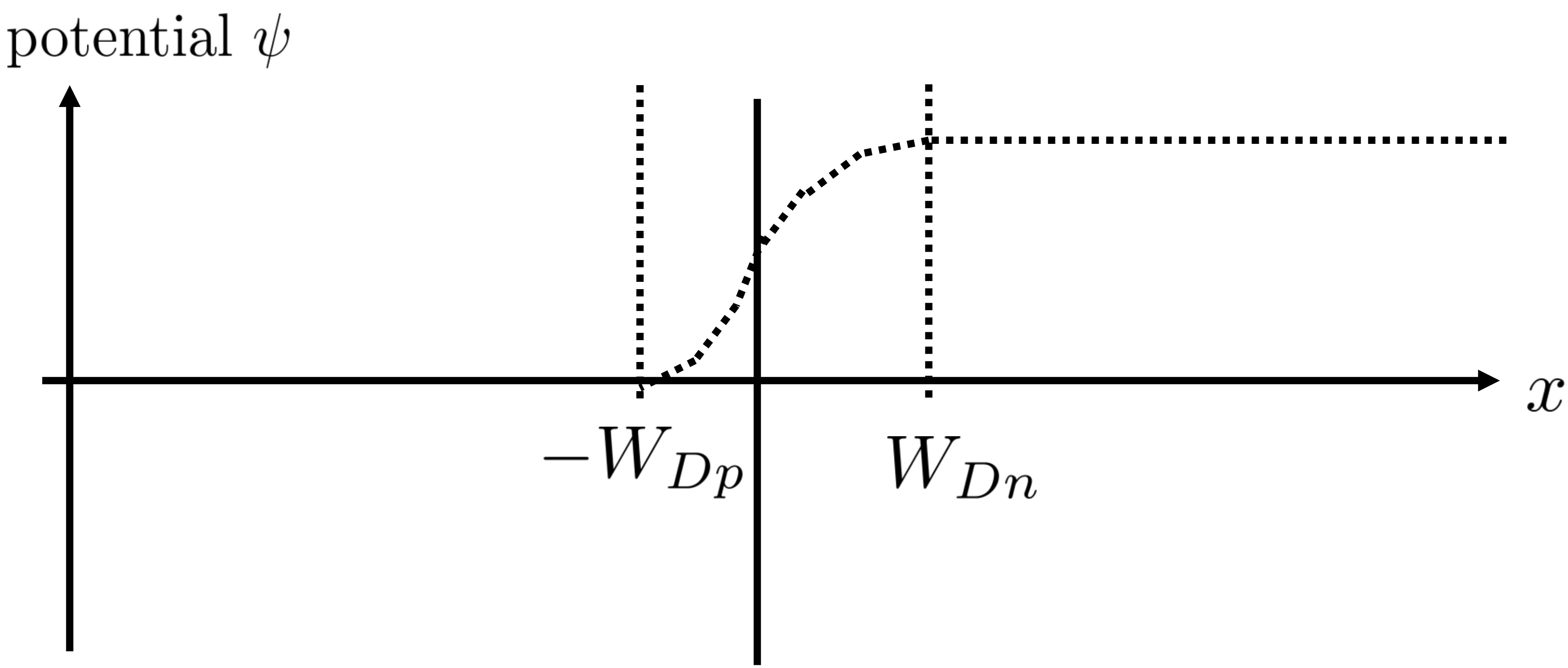
from Poisson $\frac{d\mathcal{E}}{dx} = \frac{\rho(x)}{\varepsilon_S}$

Electric field



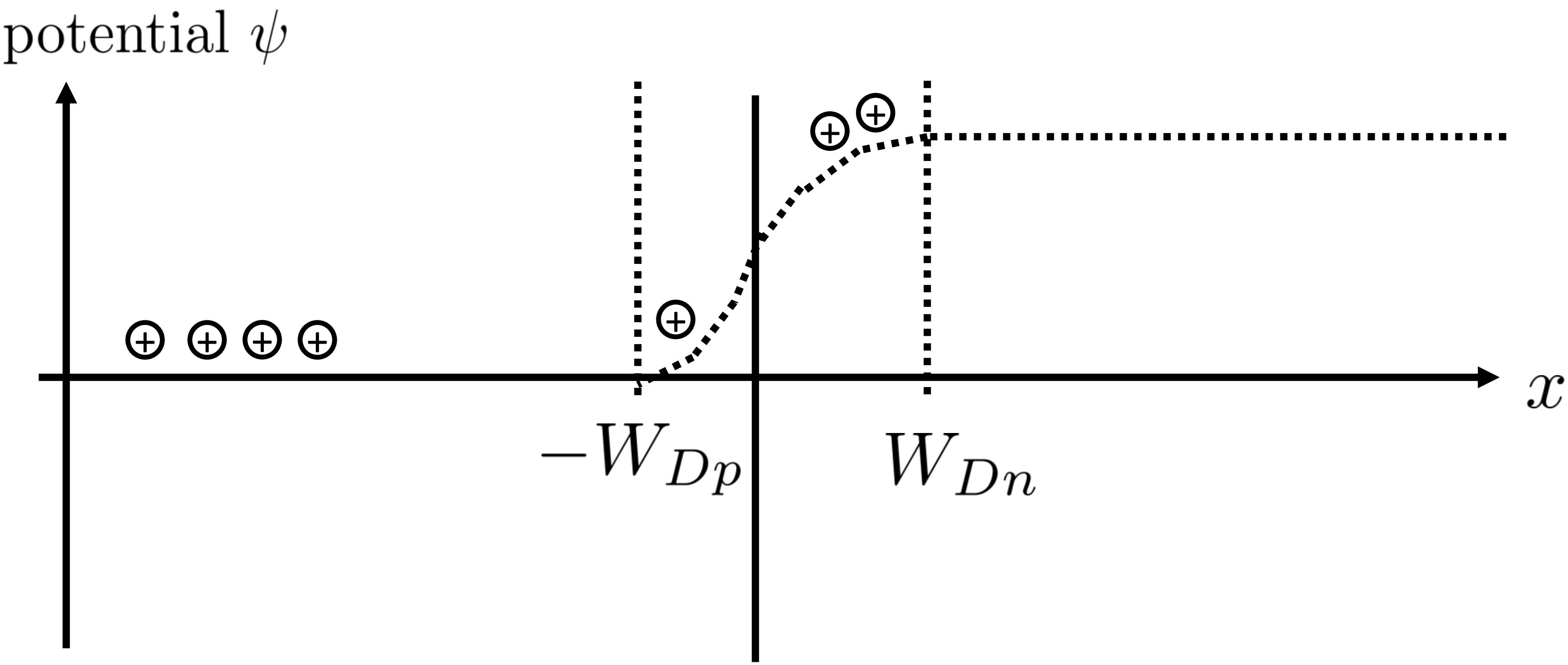
from Poisson $\frac{d\mathcal{E}}{dx} = \frac{\rho(x)}{\varepsilon_S}$

Potential



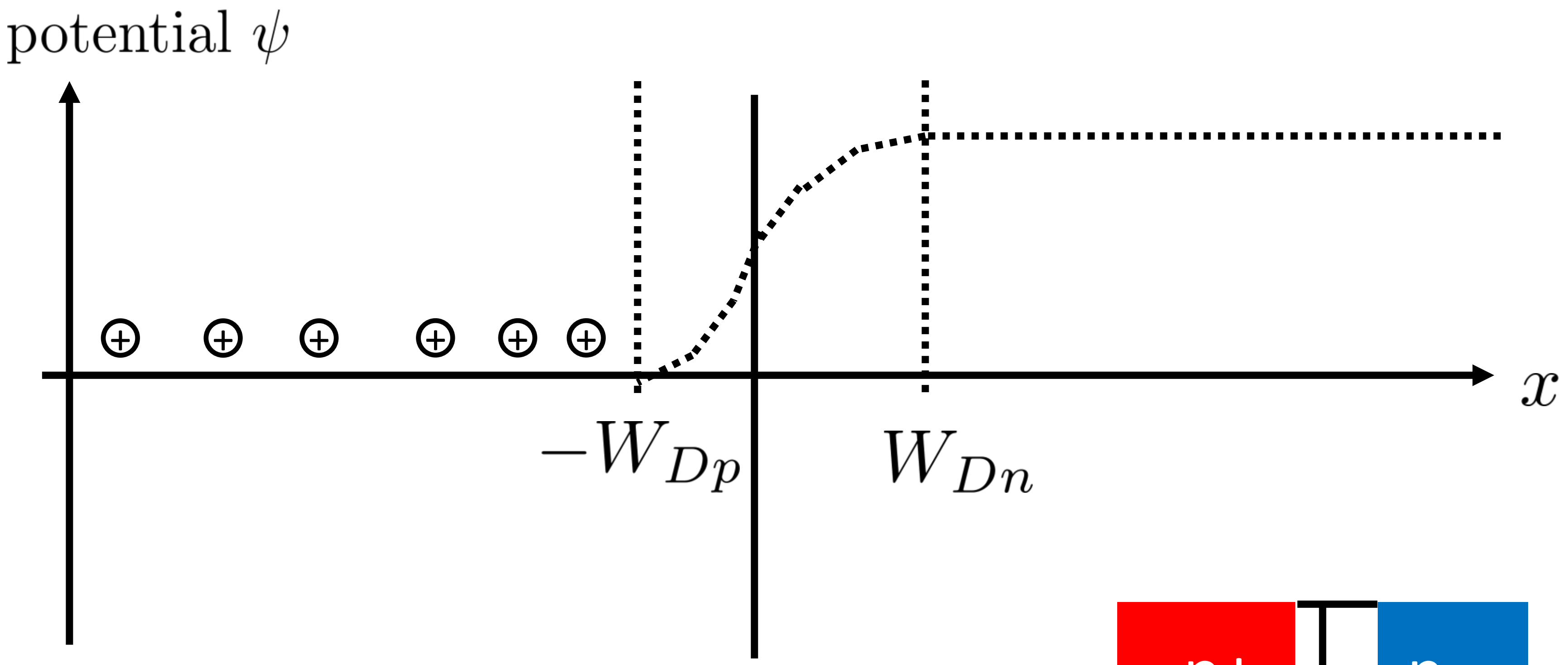
from Poisson $\frac{d\psi}{dx} = -\mathcal{E}(x)$

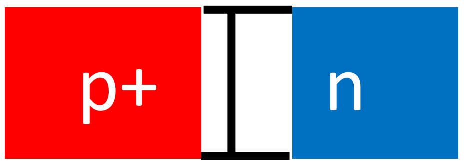
Potential



from Poisson $\frac{d\psi}{dx} = -\mathcal{E}(x)$

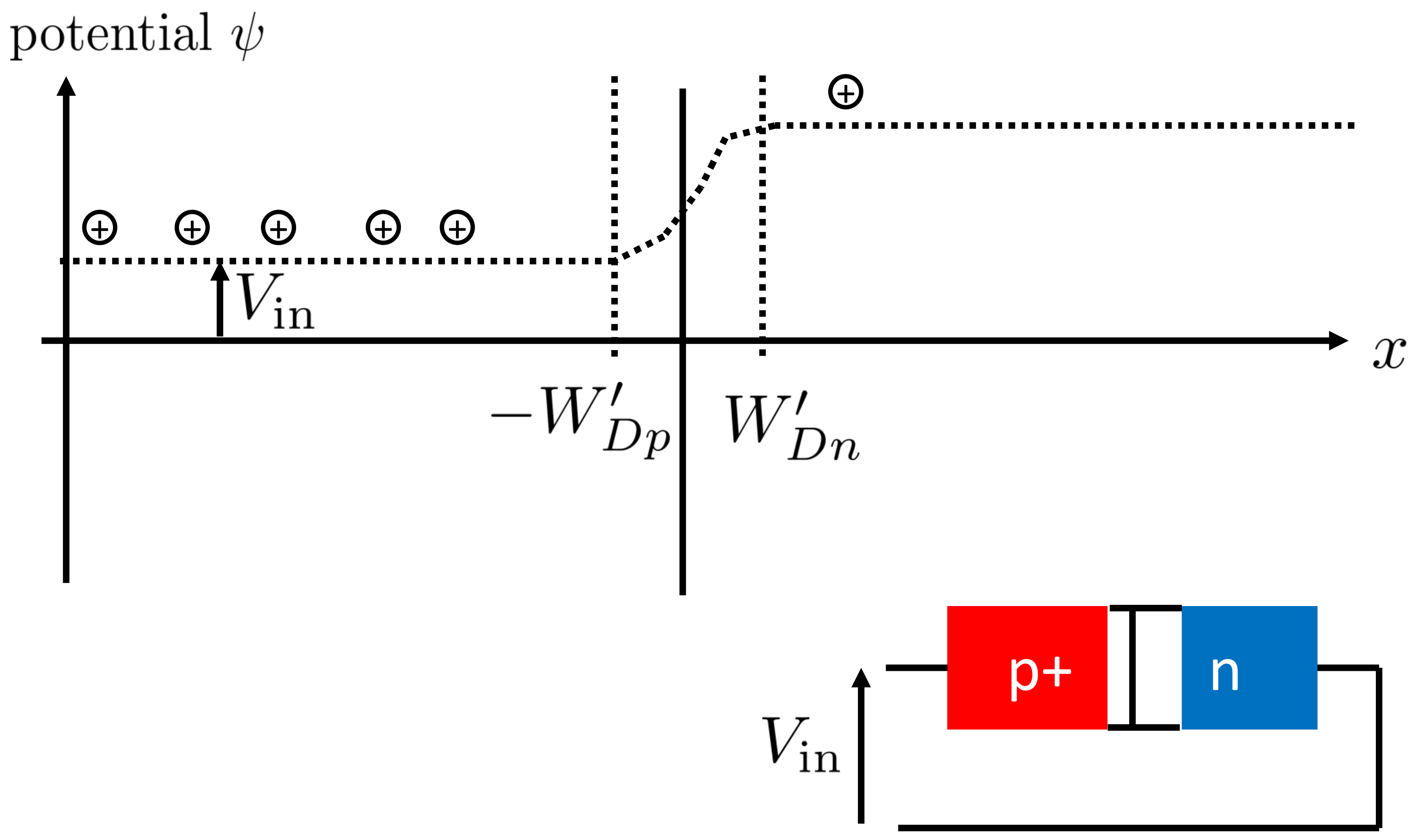
Potential



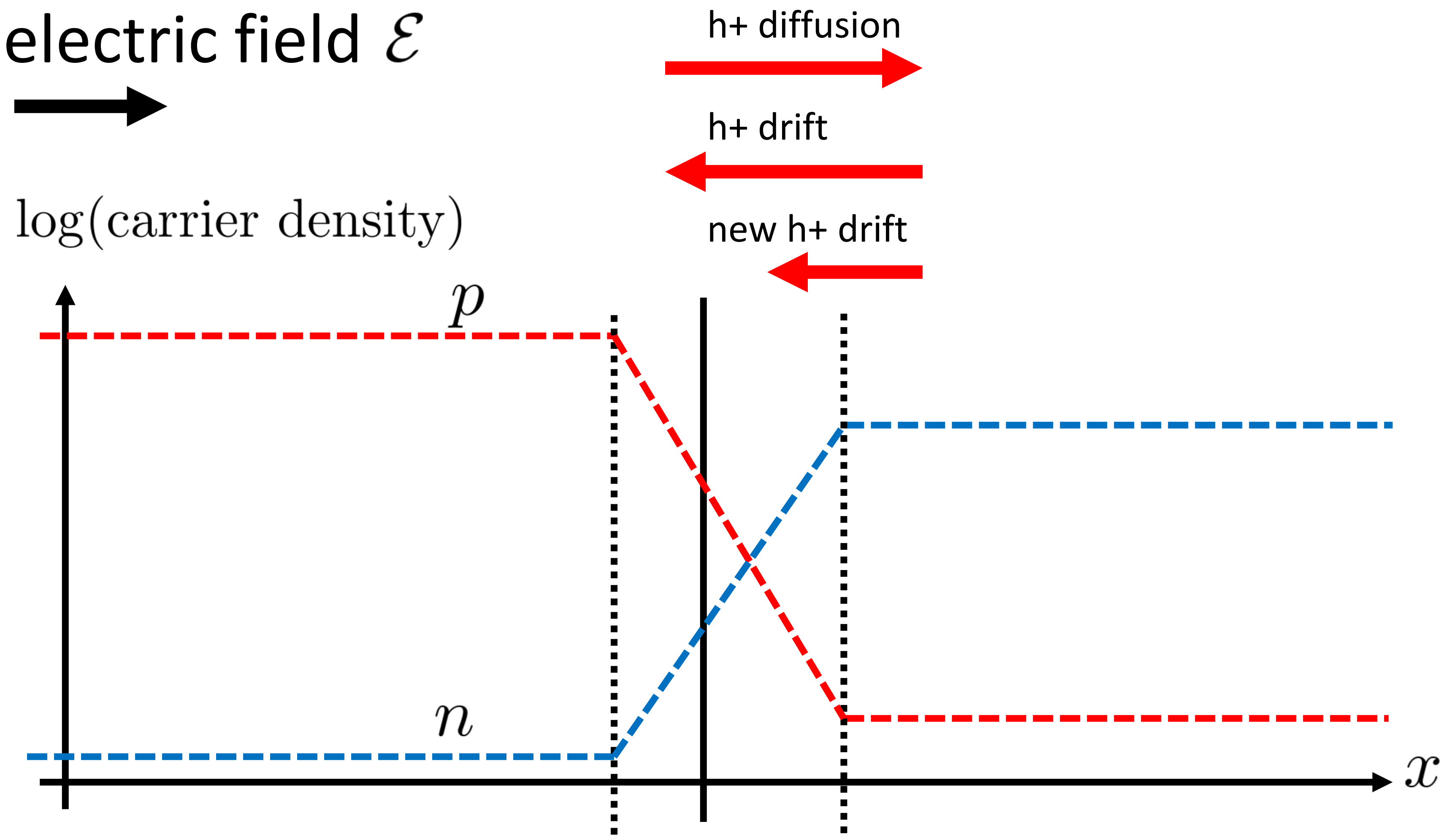


from Poisson $\frac{d\psi}{dx} = -\mathcal{E}(x)$

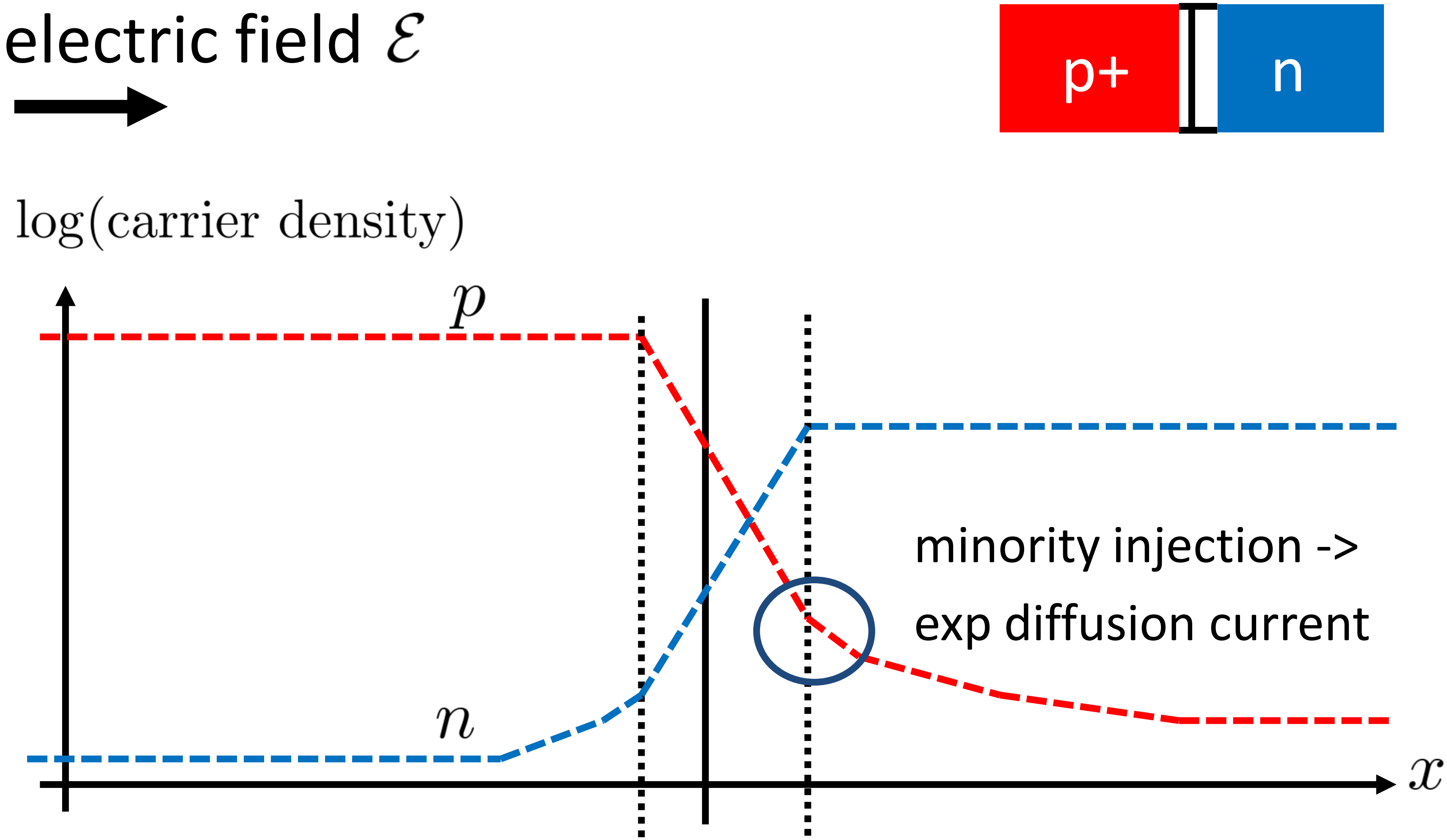
Decrease barrier



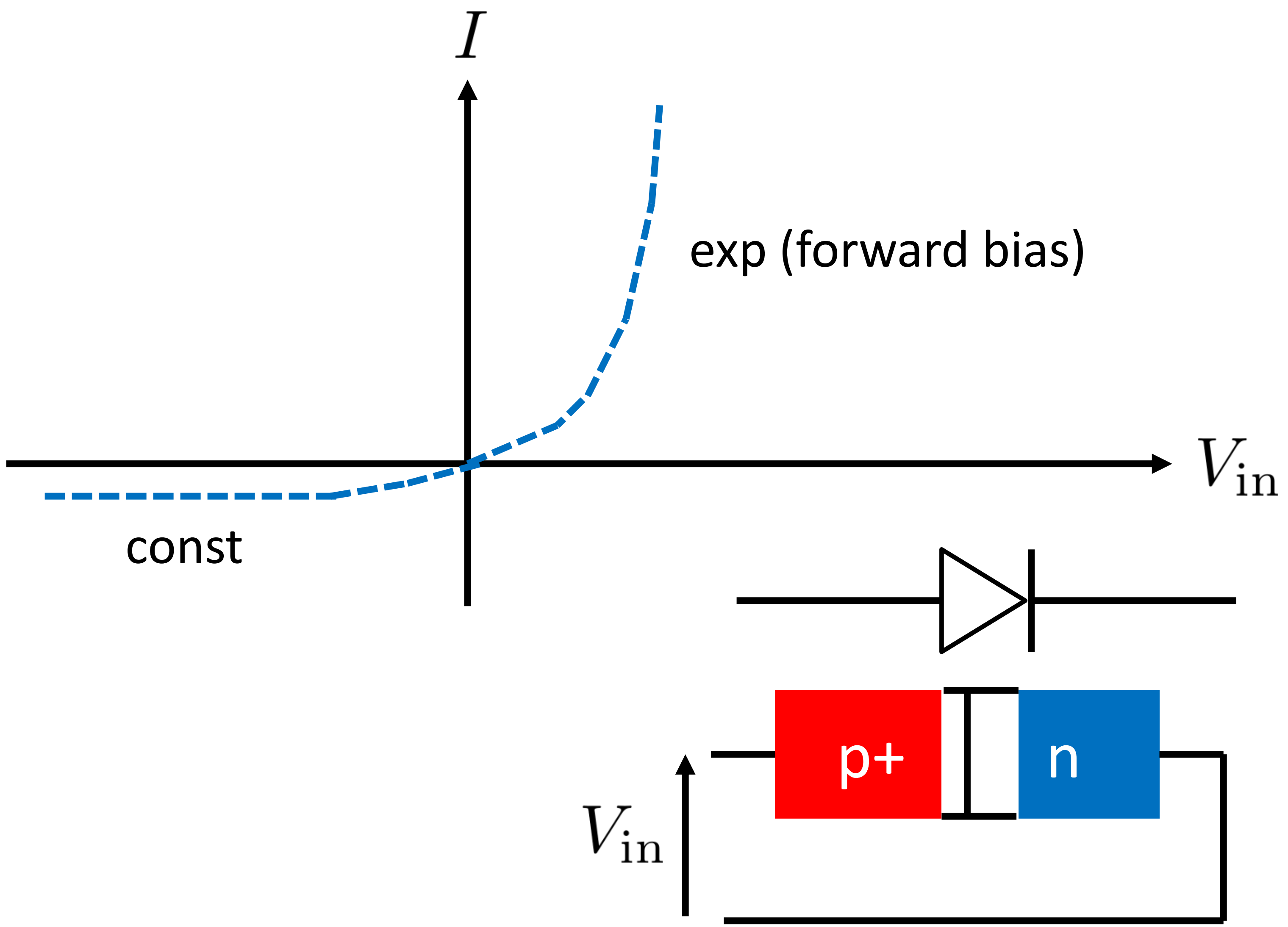
Forward bias



Forward bias

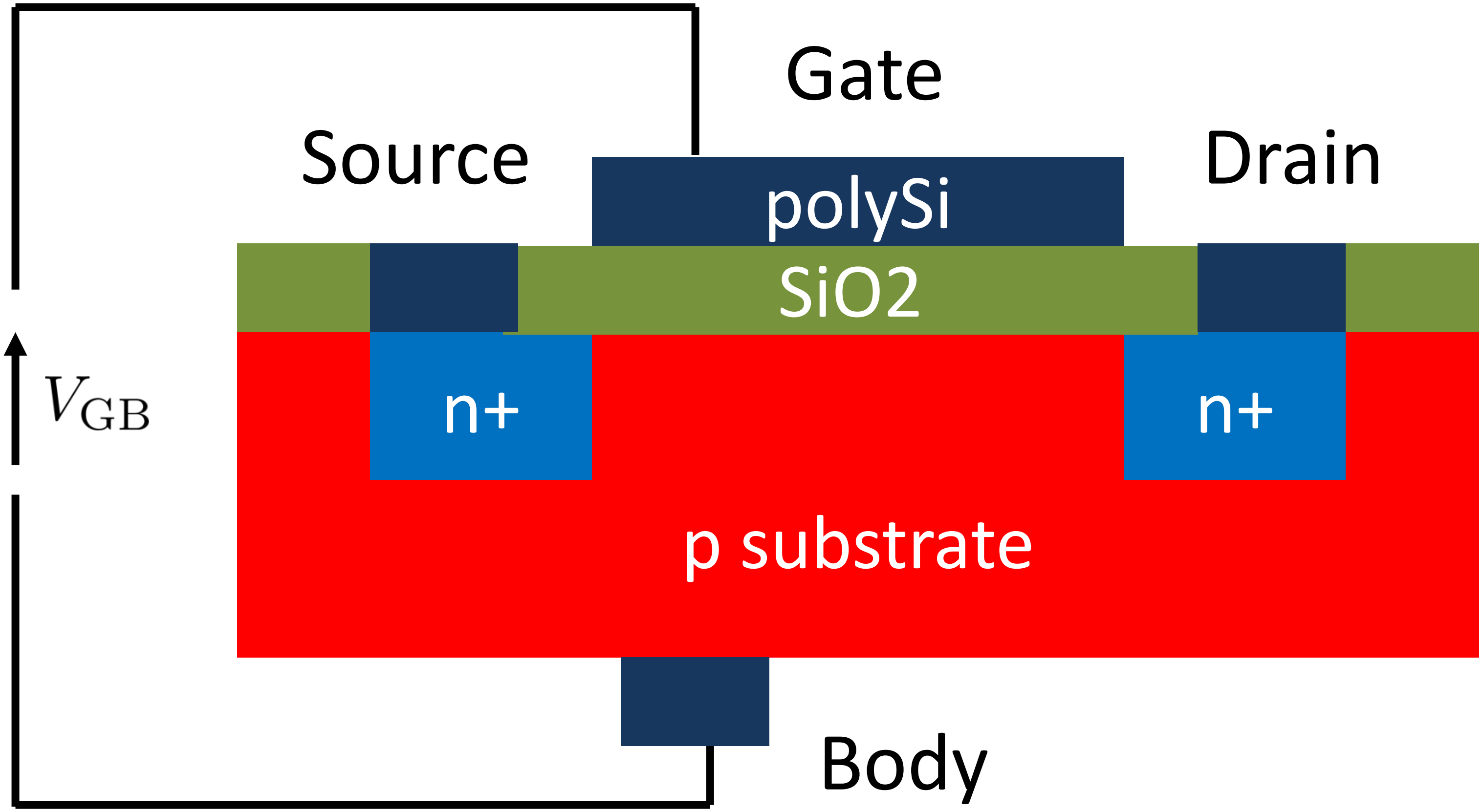


pn-junction current



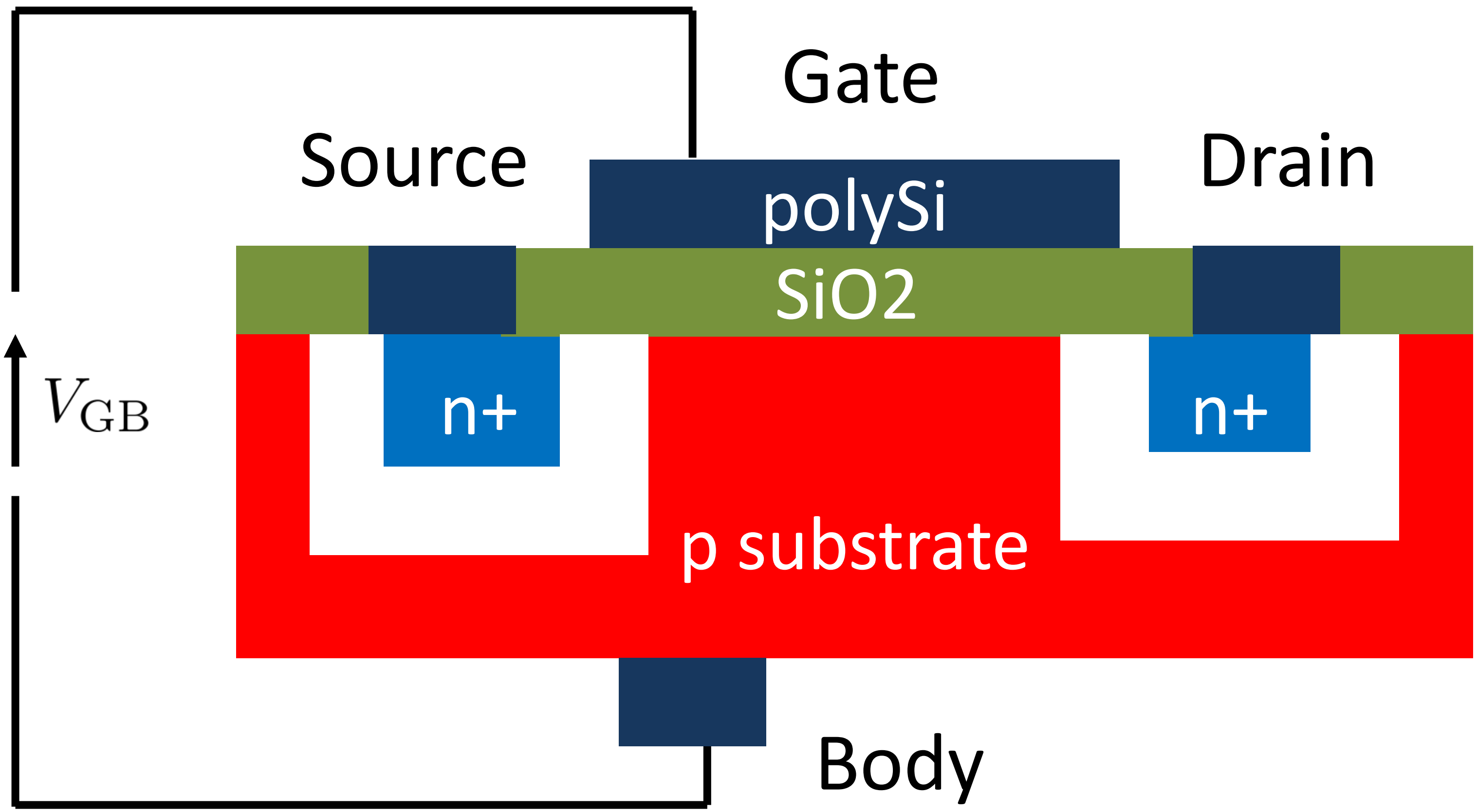
MOSFET

n (channel) MOSFET



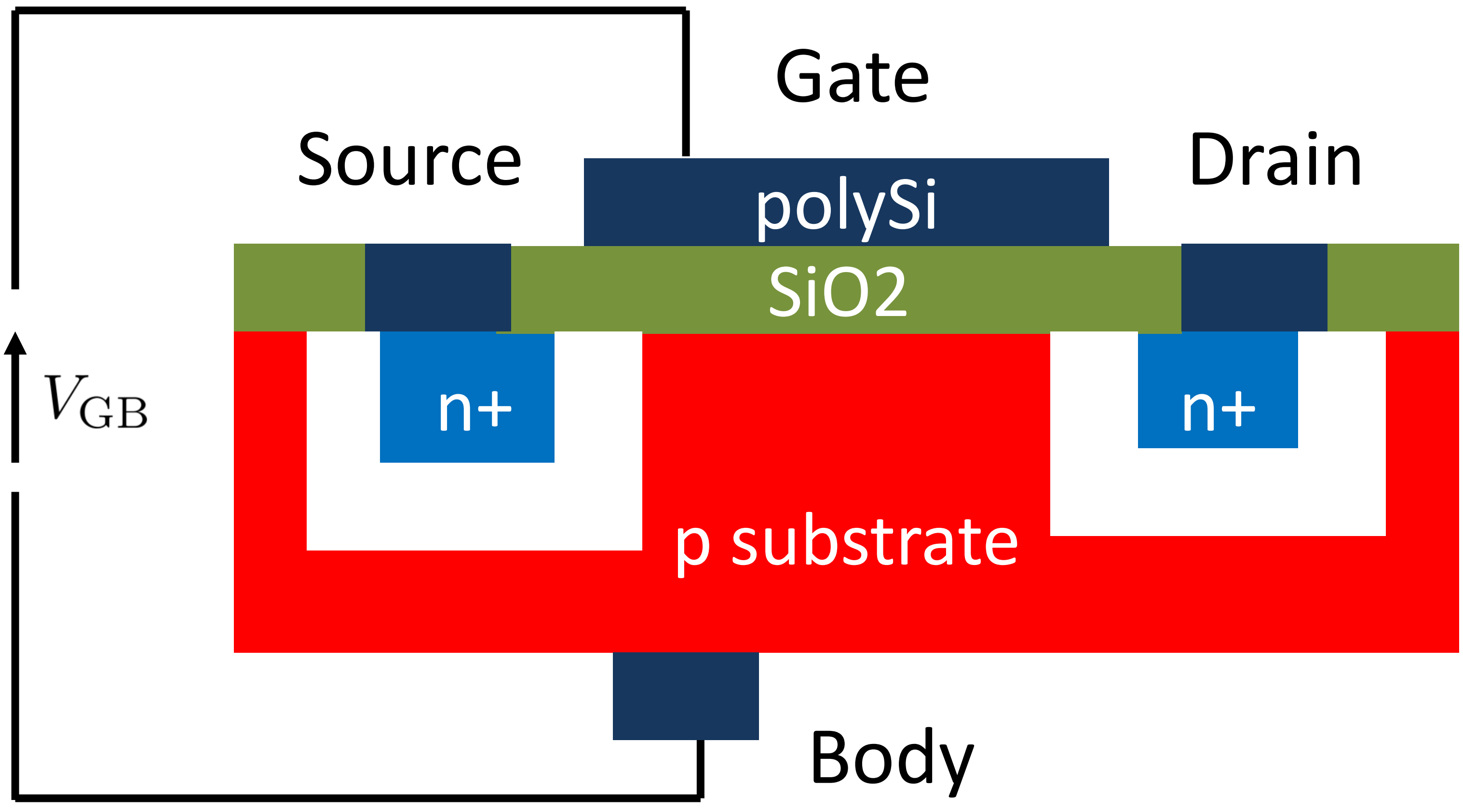
MOSFET

Two pn junctions



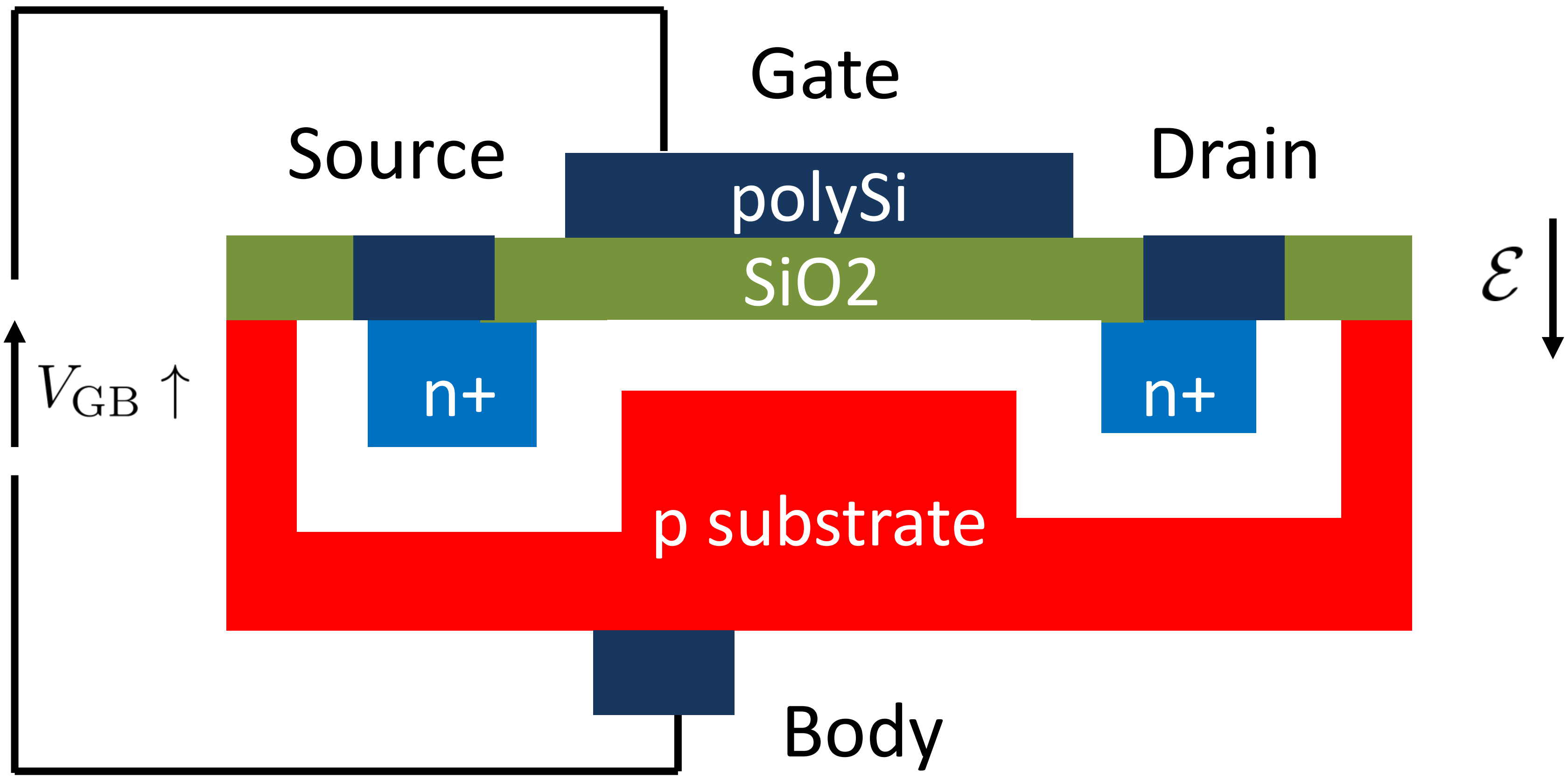
MOSFET

Two pn junctions



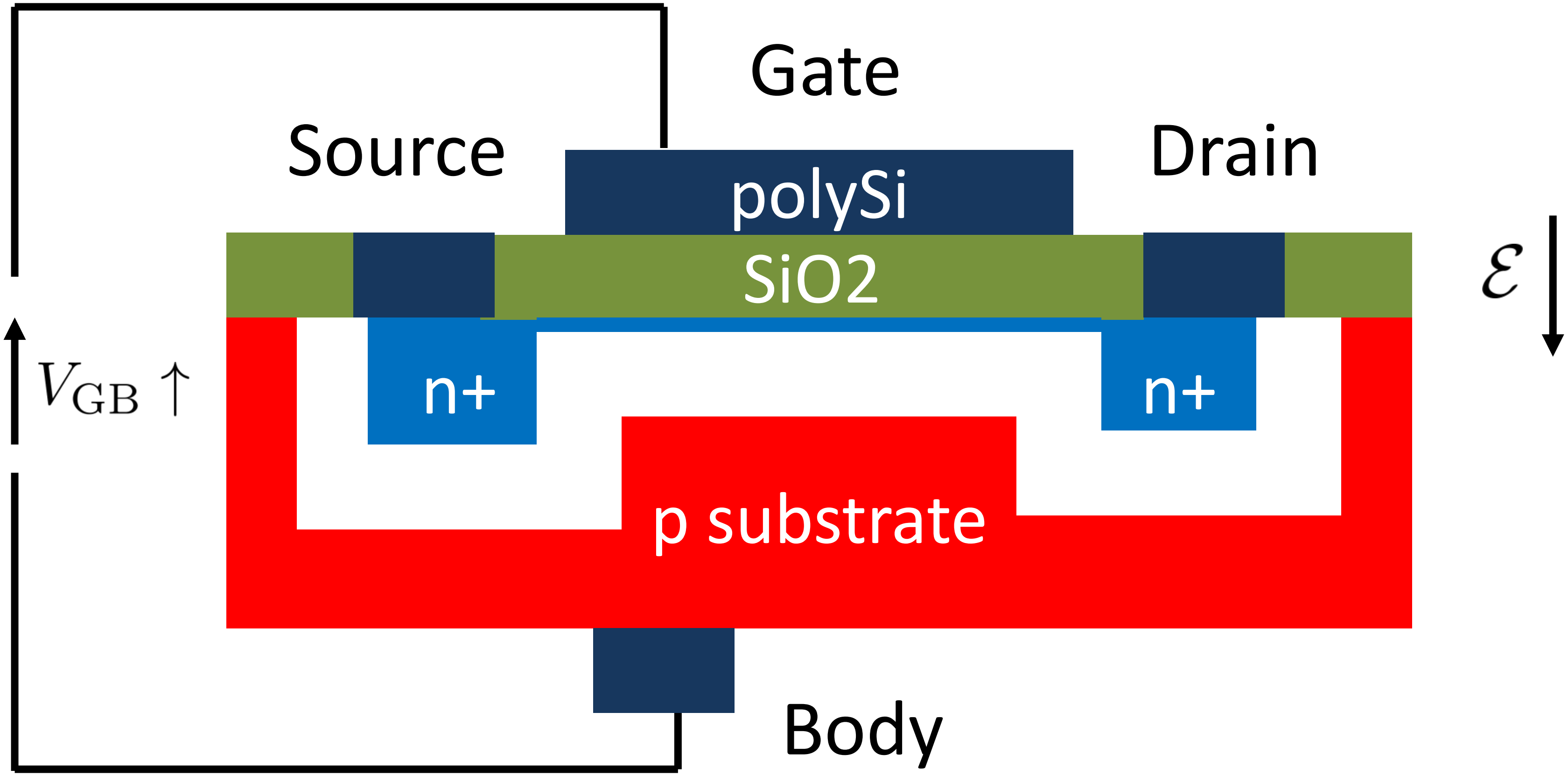
Increasing VGB...

-> Electric field -> Depletion Region



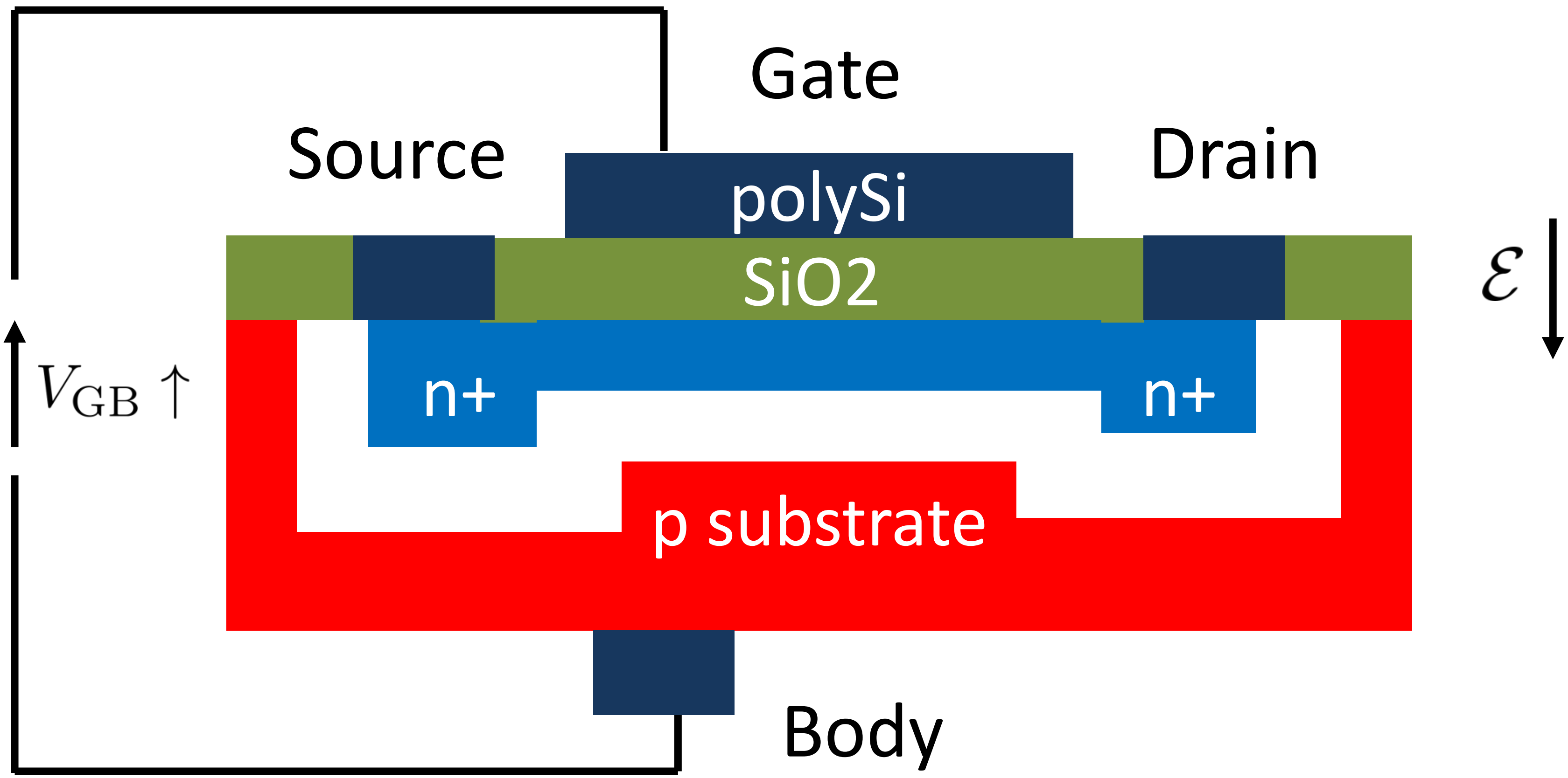
... further increasing...

-> Depletion Region & inversion starts at $V_{\mathrm{GB}} = V_{\mathrm{th}}$

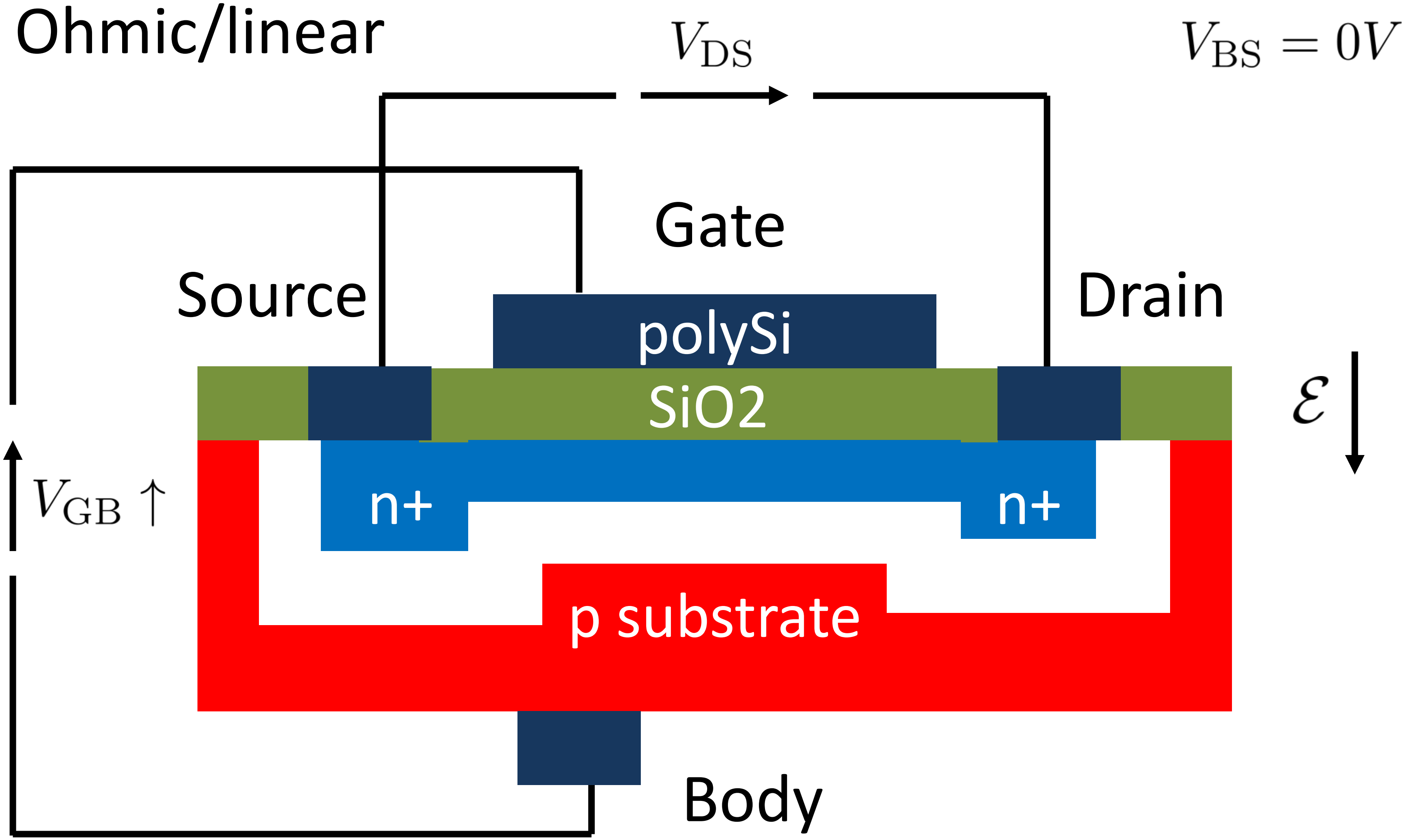


… & further increasing

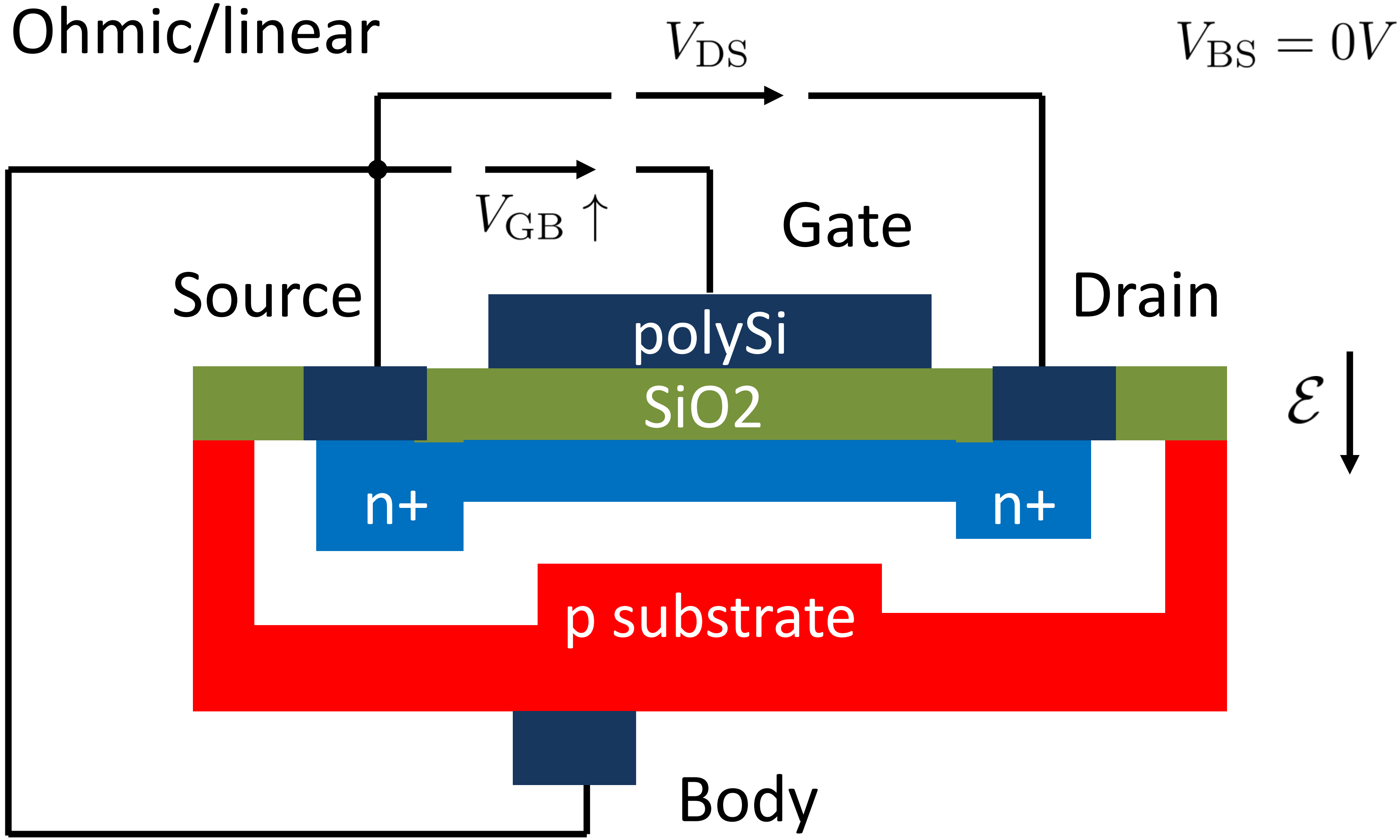
-> Inversion & n-channel forms: $V_{\mathrm{GB}} \geq V_{\mathrm{th}}$



MOSFET

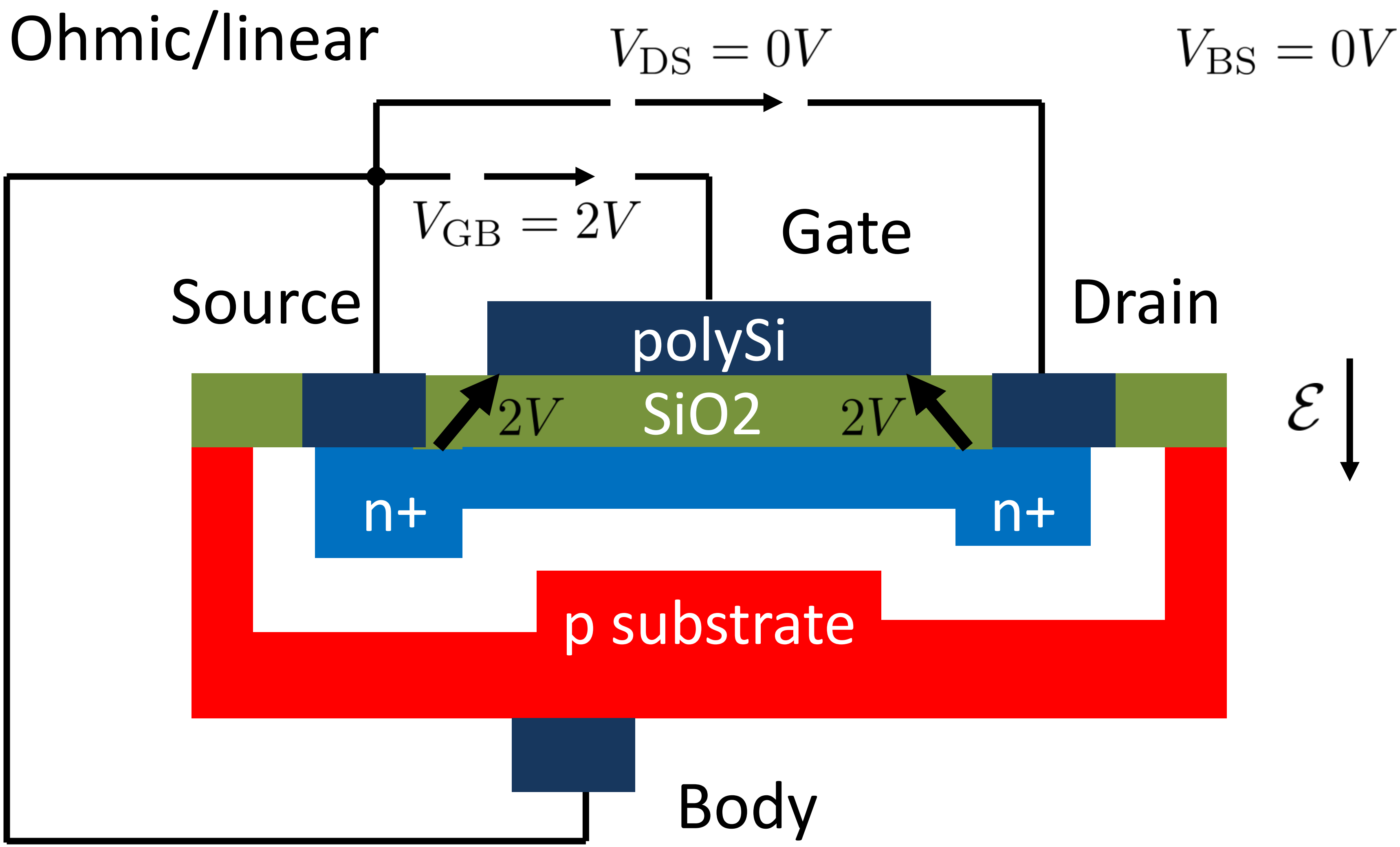

Ohmic/linear
V_{DS}
$V_{\mathrm{BS}} = 0V$
Gate
Source
Drain
polySi
SiO2
$\mathcal{E}$
$V_{\mathrm{GB}} \uparrow$
n+
n+
p substrate
Body

MOSFET

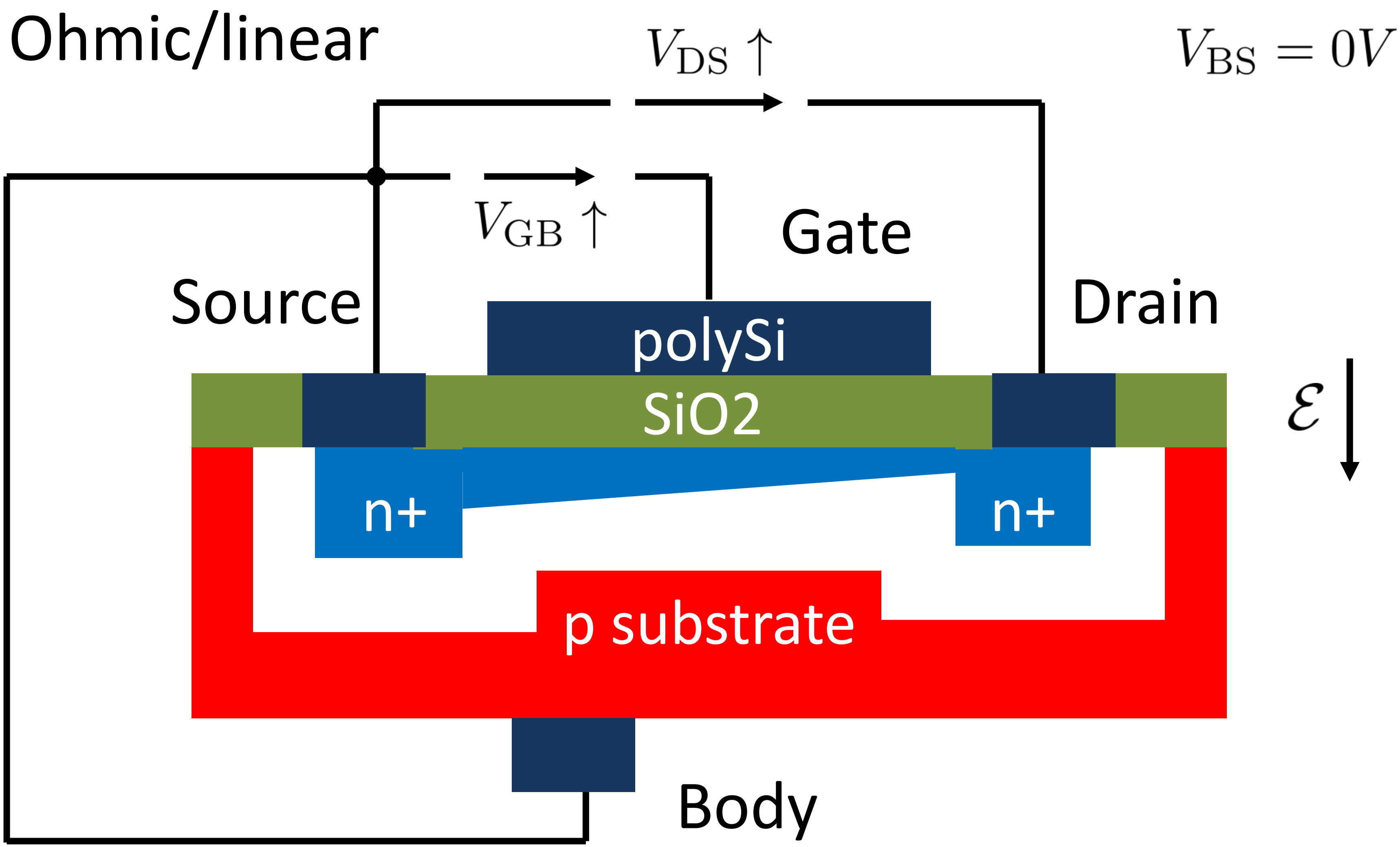


Ohmic/linear
V_{DS}
$V_{\mathrm{BS}} = 0V$
$V_{\mathrm{GB}} \uparrow$
Gate
Source
Drain
polySi
SiO2
$\mathcal{E}$
n+
n+
p substrate
Body

MOSFET – channel potential

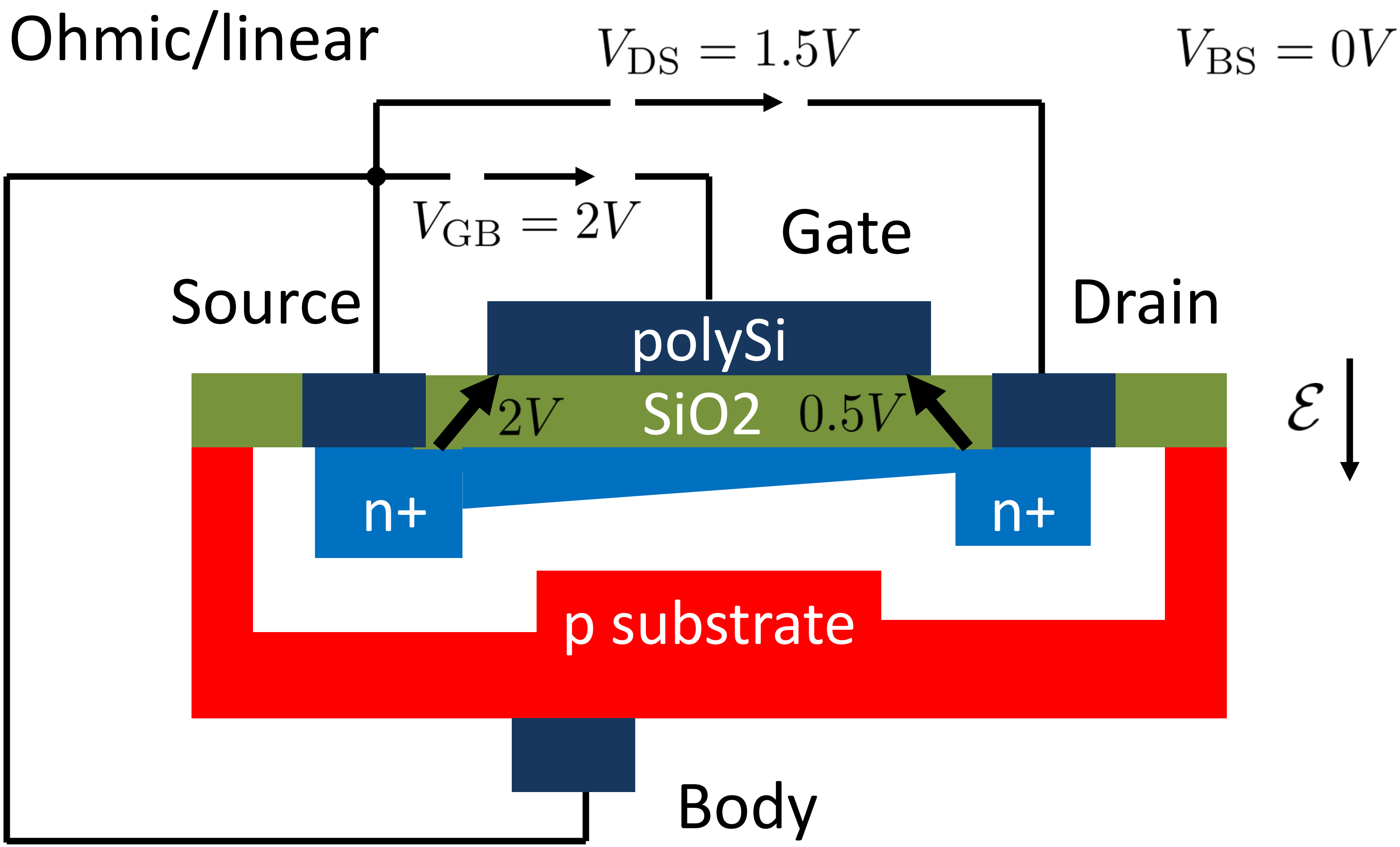


MOSFET

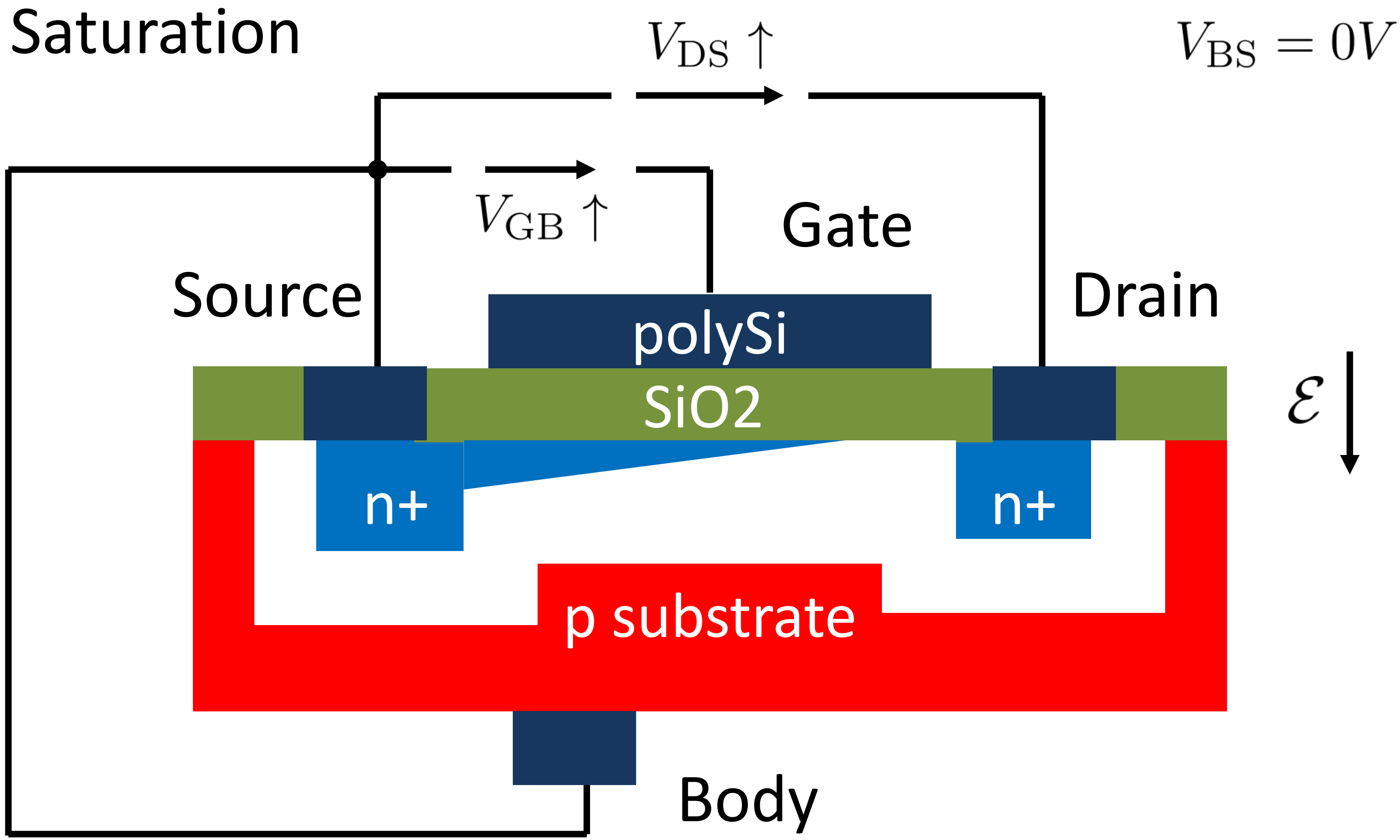


Ohmic/linear
$V_{\mathrm{DS}} \uparrow$
$V_{\mathrm{BS}} = 0V$
$V_{\mathrm{GB}} \uparrow$
Gate
Source
Drain
polySi
SiO2
$\mathcal{E}$
n+
n+
p substrate
Body

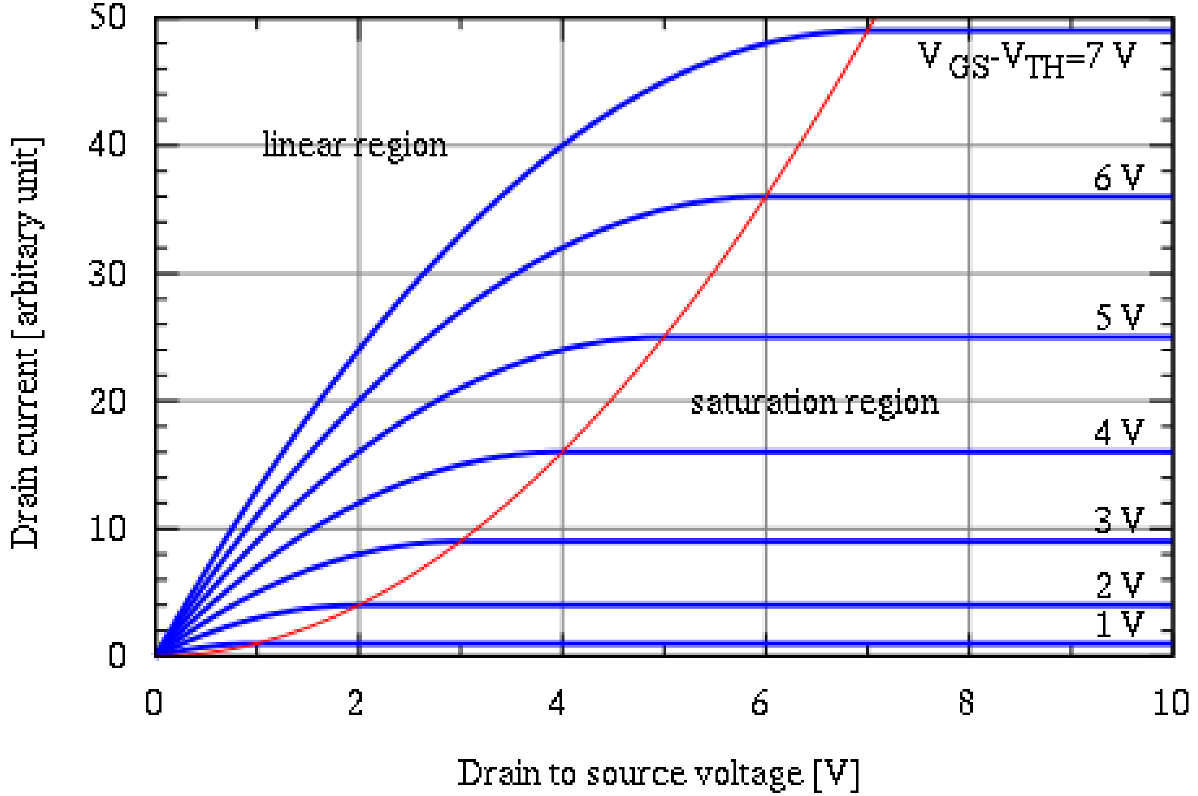
MOSFET – channel shape



MOSFET


Saturation
$V_{\text{DS}} \uparrow$
$V_{\text{BS}} = 0V$
$V_{\text{GB}} \uparrow$
Gate
Source
Drain
polySi
SiO2
$\mathcal{E}$
n+
n+
p substrate
Body

MOSFET



calculated, from commons.wikimedia.org/wiki/File:IvsV_mosfet.svg#/media/File:IvsV_mosfet.svg