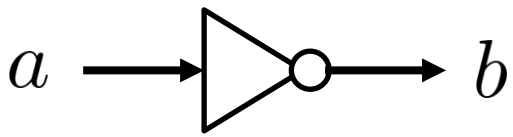
# Beyond classical circuit design lecture 8

## CMOS Synthesis

# Further Reading

Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic: *Digital Integrated Circuits. A Design Perspective. 2nd edition.* Prentice Hall, 2003.

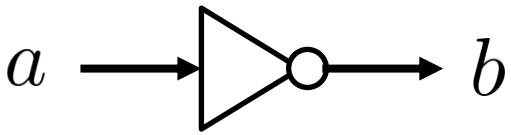
# Back to synthesis...




$$a \rightarrow b \downarrow$$

$$\neg a \rightarrow b \uparrow$$

# Back to synthesis...

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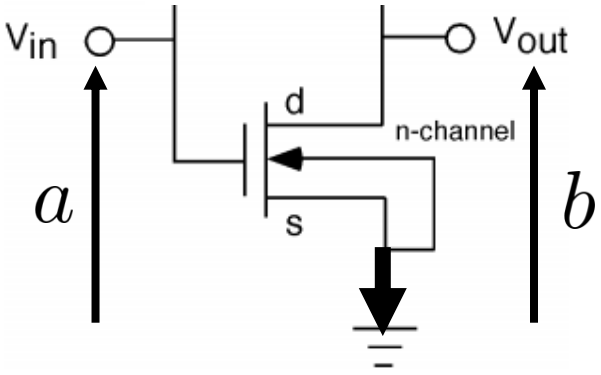


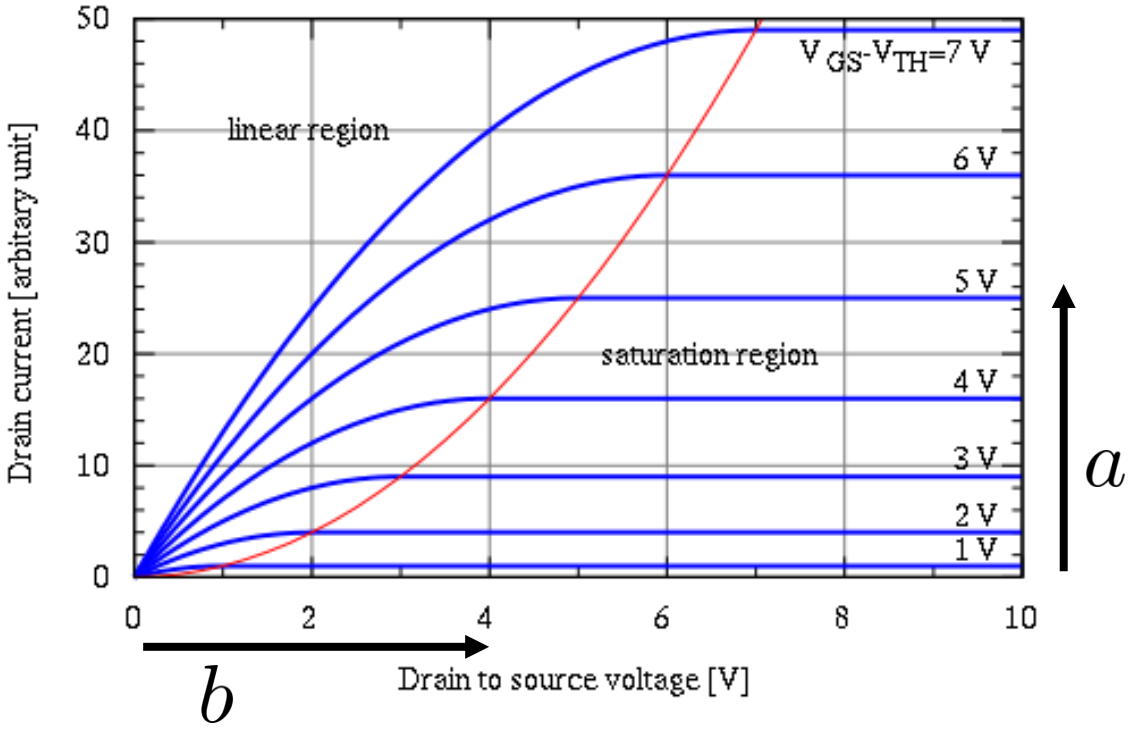


L: by Bill Wilson, cnx.org/contents/013d787f-9a59-4567-be18-9c83eac6d884@1/CMOS_Logic

R: commons.wikimedia.org/wiki/File:IvsV_mosfet.svg#/media/File:IvsV_mosfet.svg

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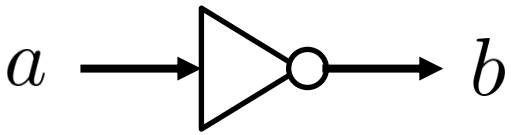


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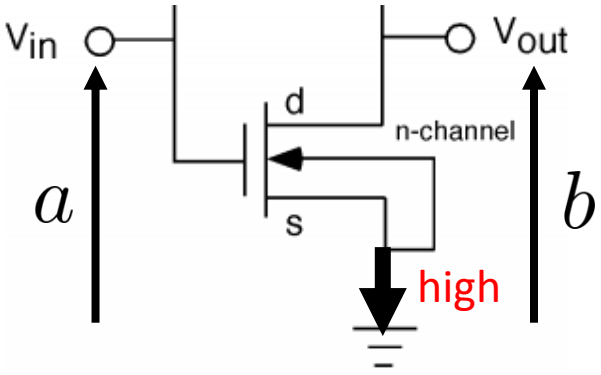


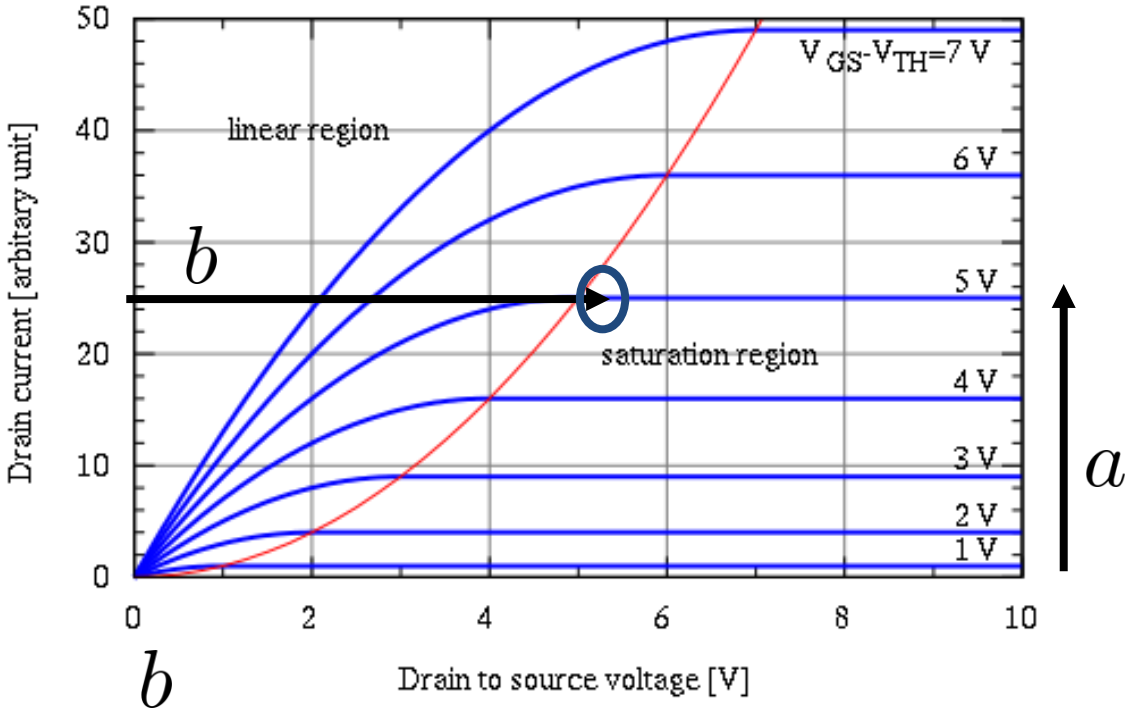


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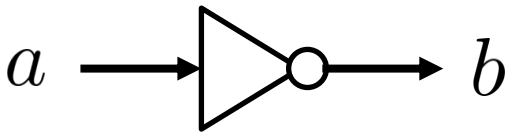


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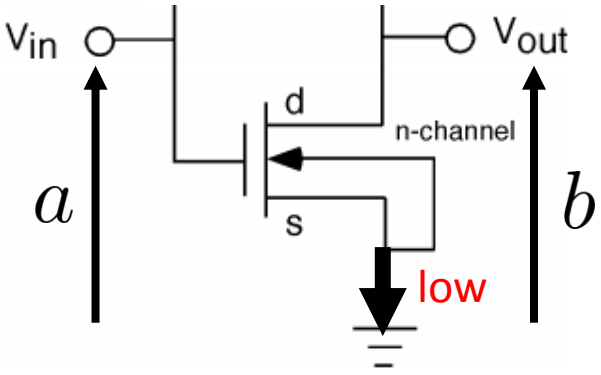


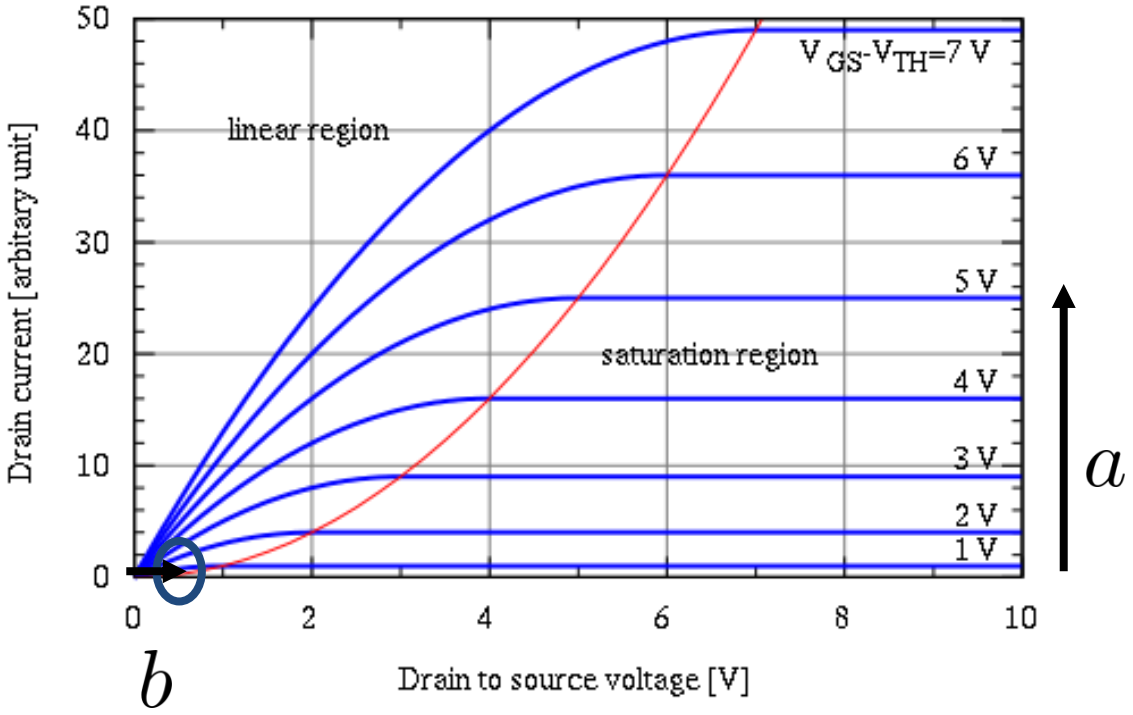


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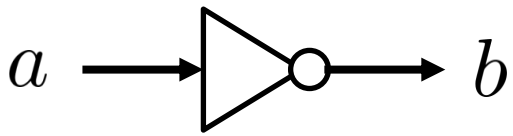


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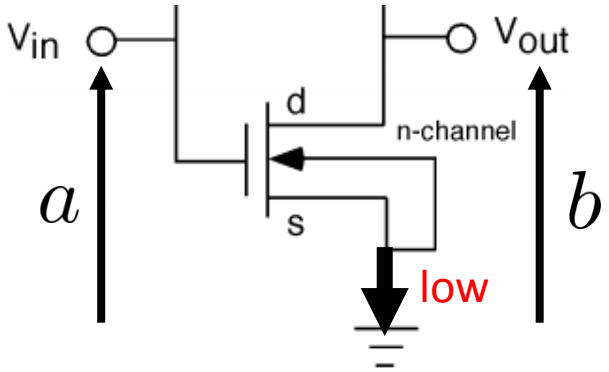



low a ->

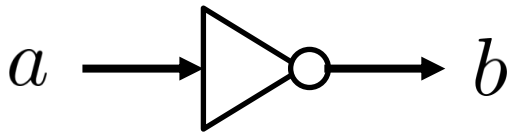
nFET in cutoff region

high a ->

nFET in ohmic region

by Bill Wilson, cnx.org/contents/013d787f-9a59-4567-be18-9c83eac6d884@1/CMOS_Logic

# Back to synthesis...

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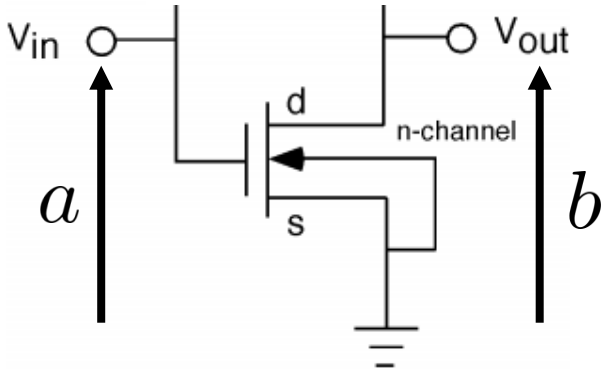


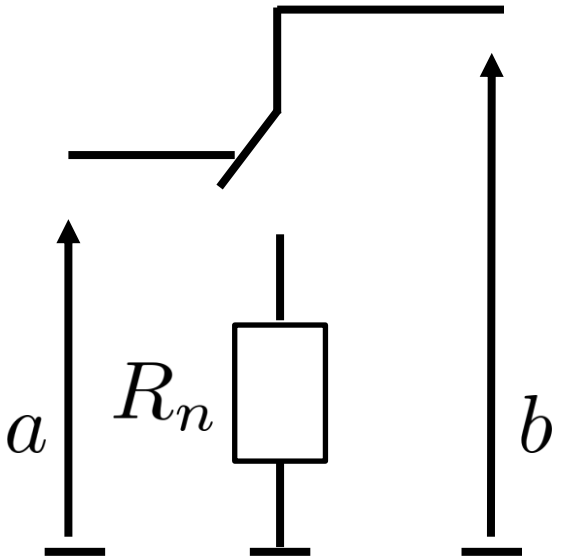


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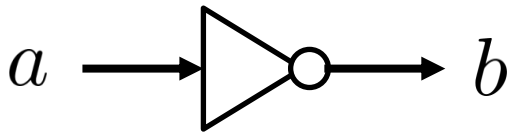


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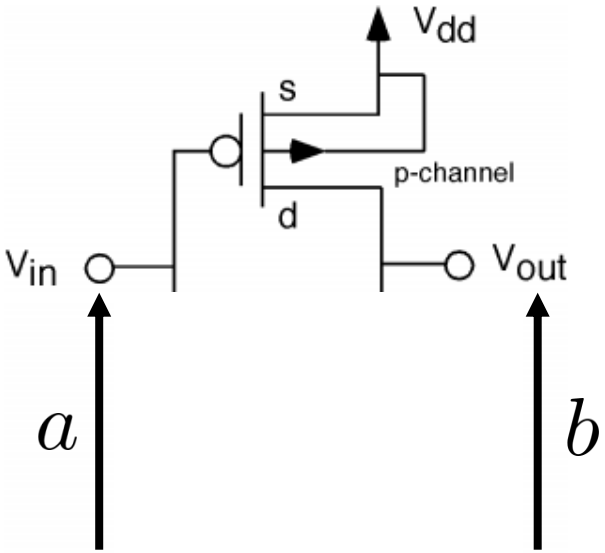


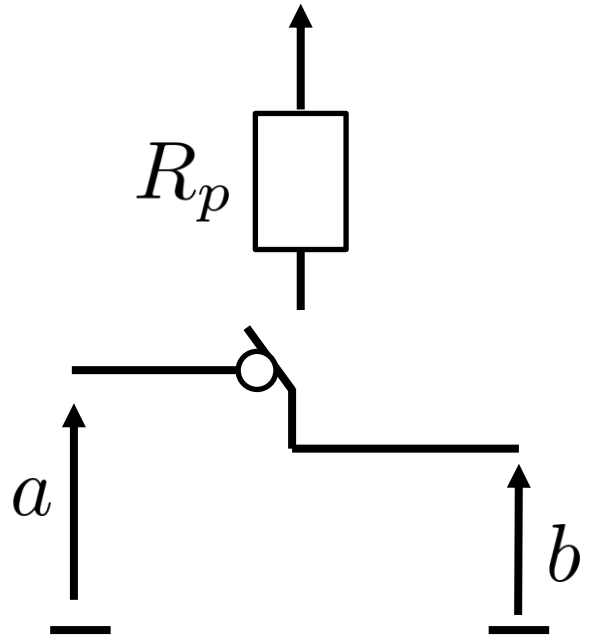


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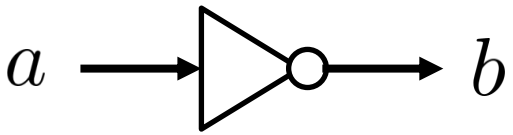
# Putting it together

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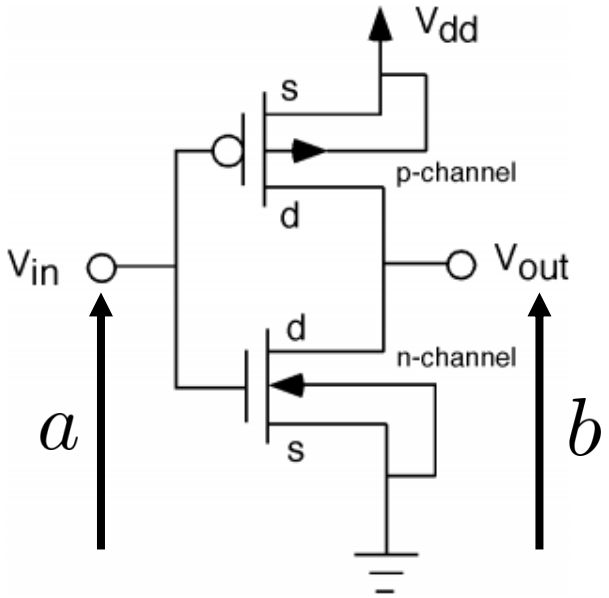
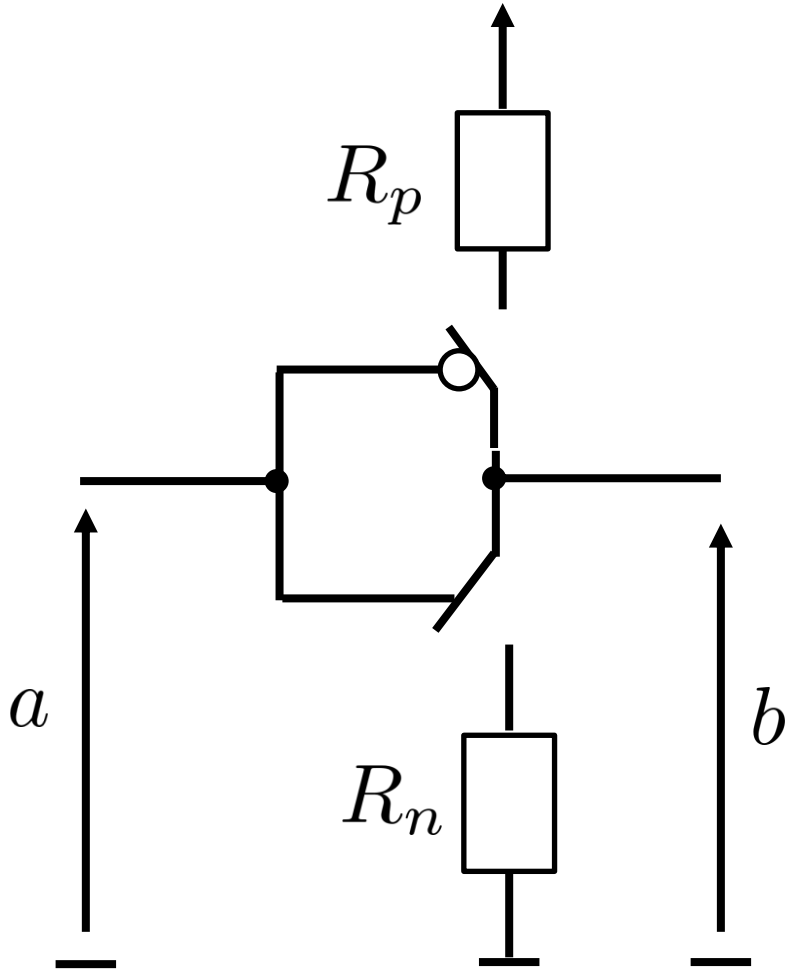


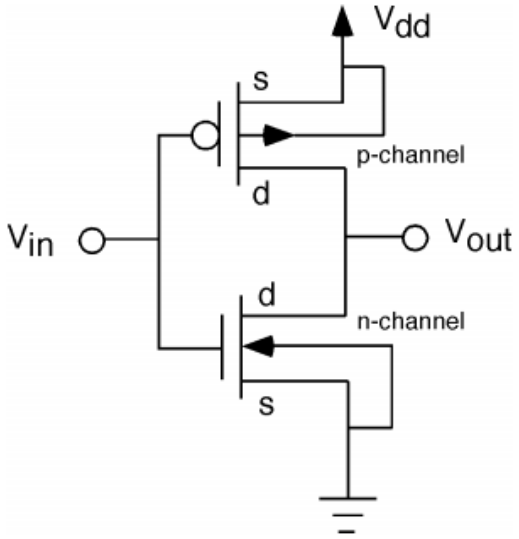

by Bill Wilson, cnx.org/contents/013d787f-9a59-4567-be18-9c83eac6d884@1/CMOS_Logic

# CMOS Inverter – switch model

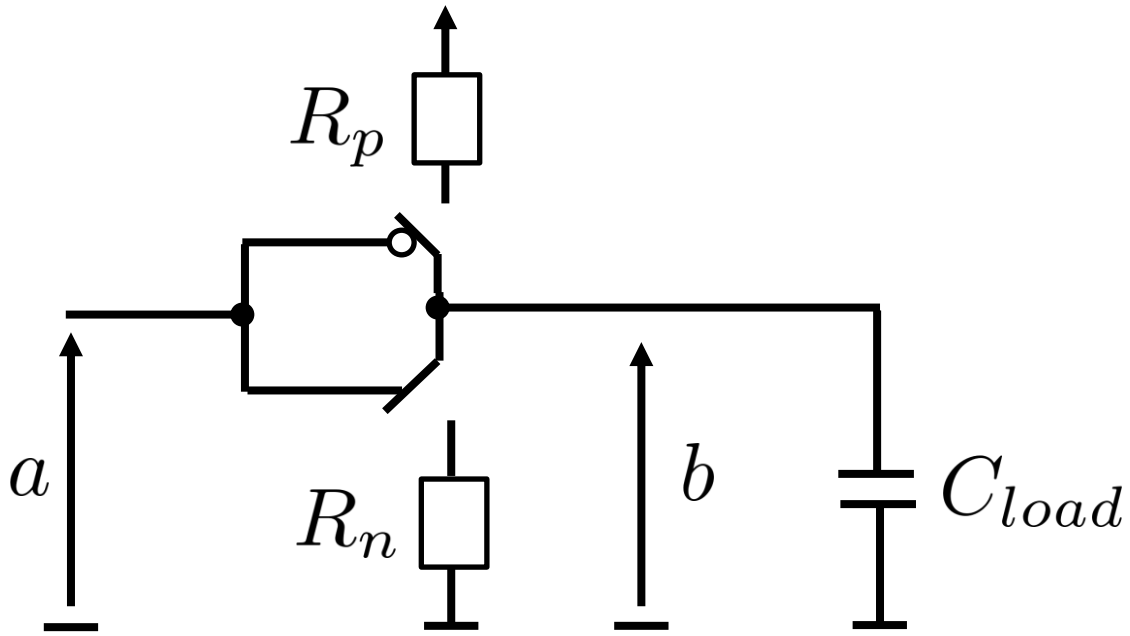


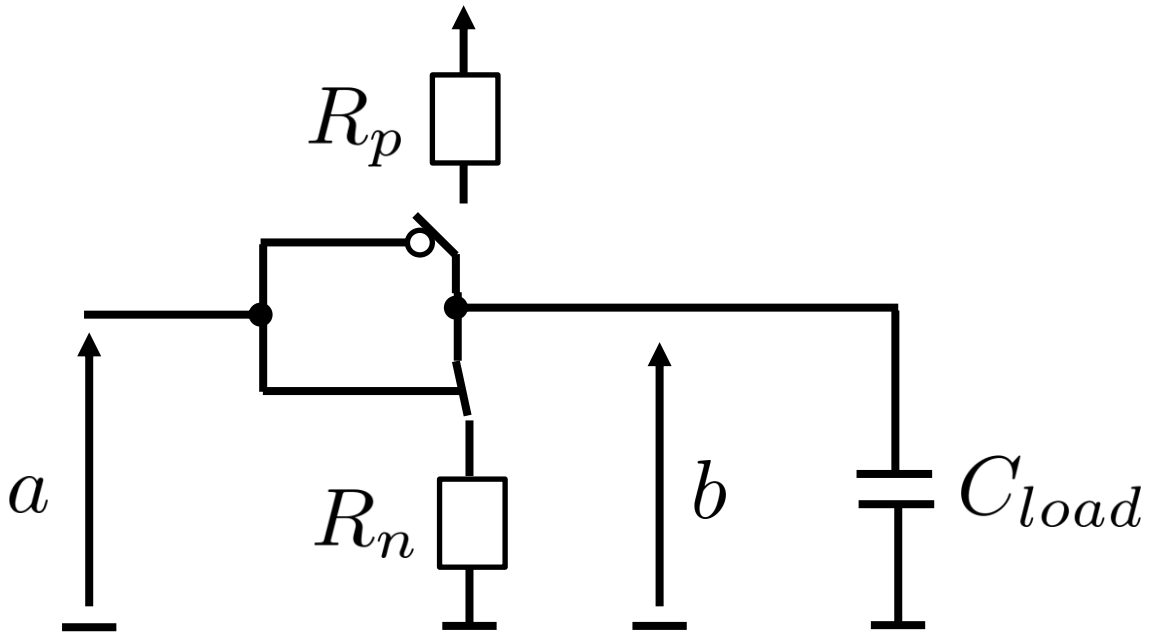

Transistor sizing

$$R \propto L/W$$

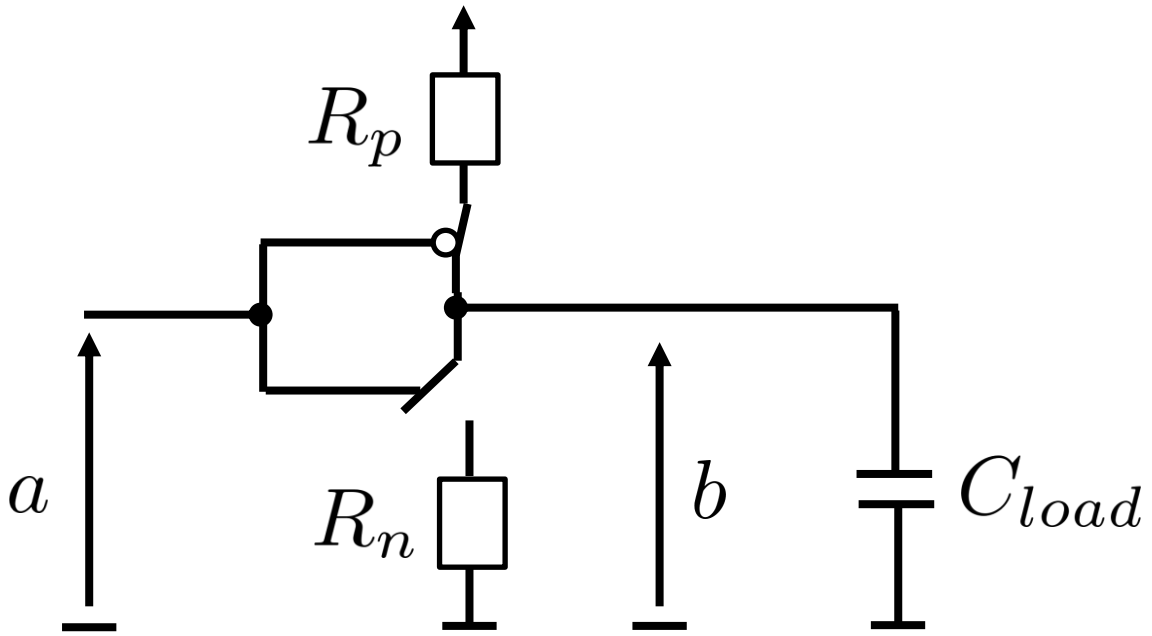


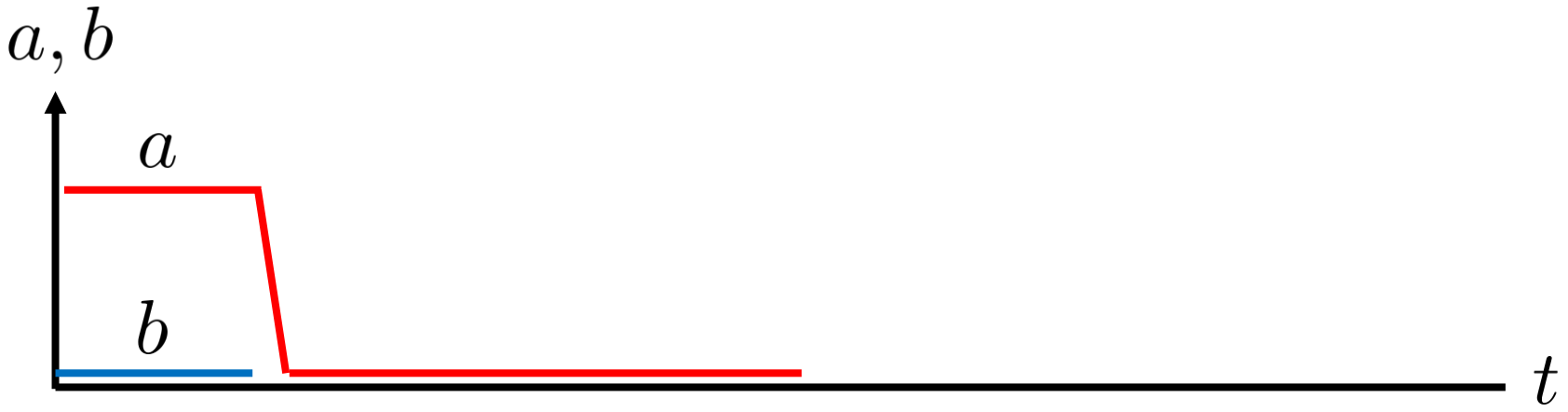
# CMOS Inverter – switch transient

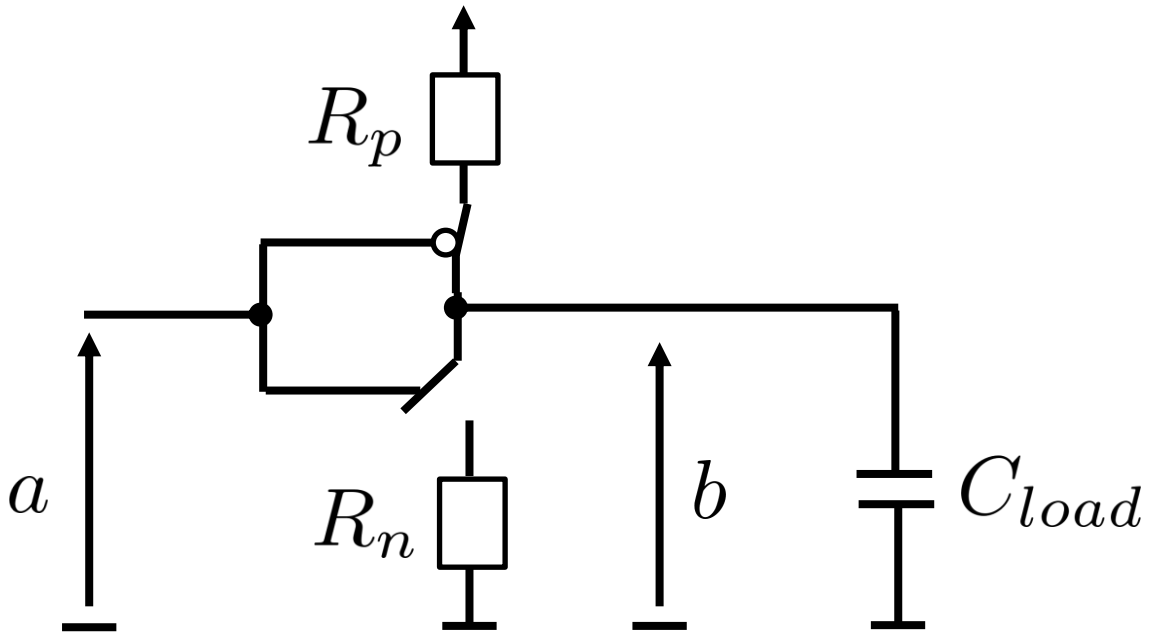


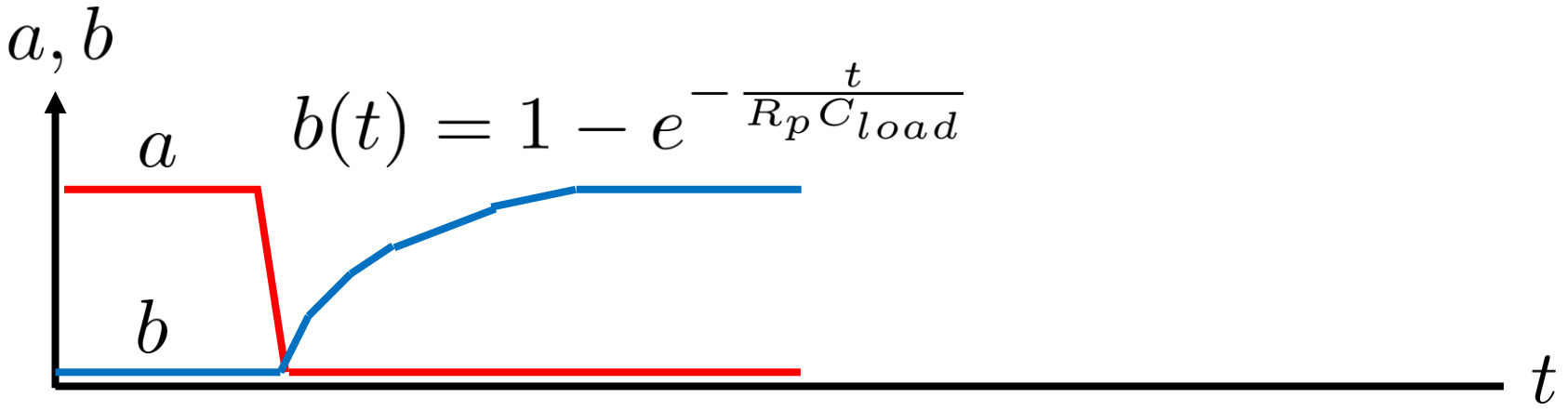

$R_p$
$a$
$R_n$
$b$
$C_{load}$

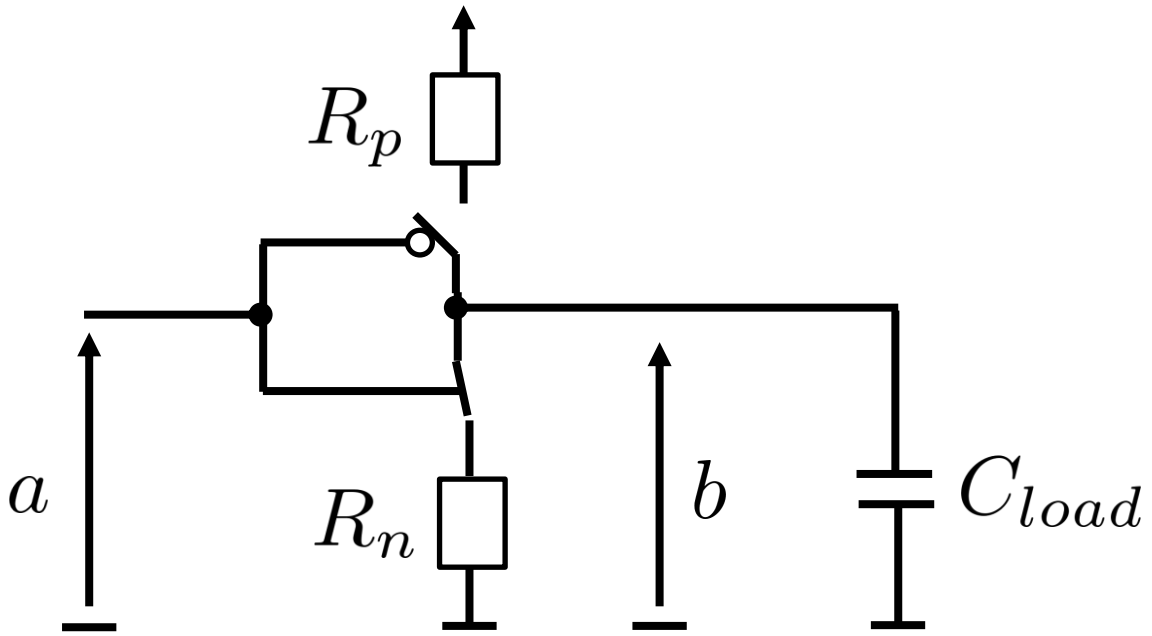

$a, b$
$a$
$b$
$t$

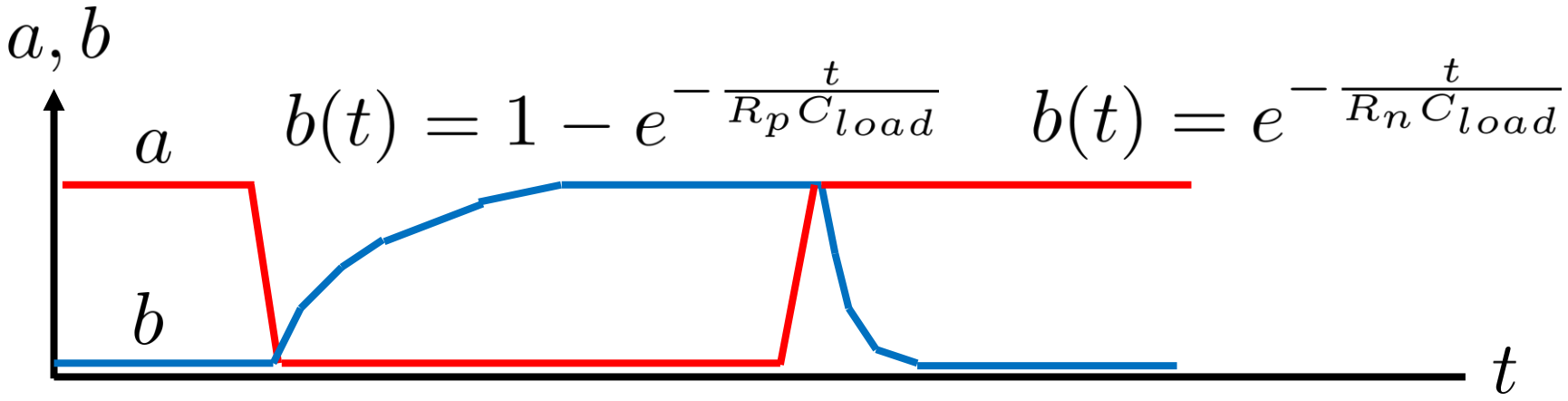

$R_p$
$a$
$R_n$
$b$
$C_{load}$


$a, b$
$a$
$b$
$t$

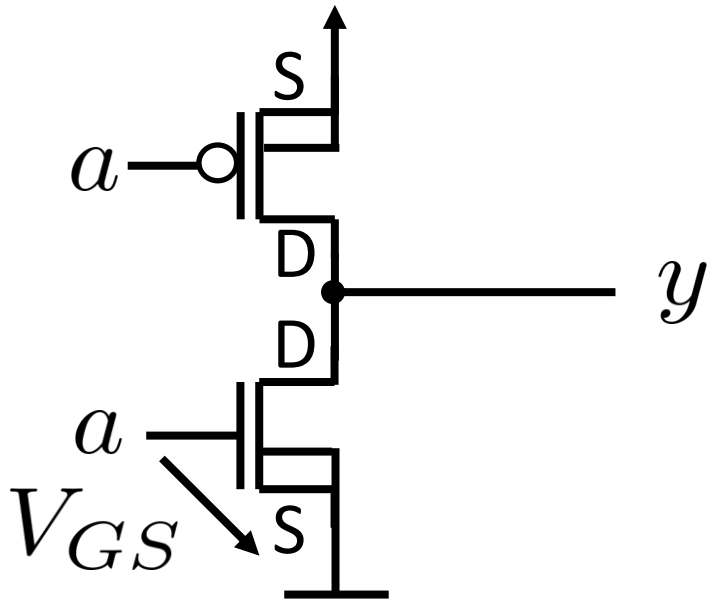

$R_p$
$a$
$R_n$
$b$
$C_{load}$


$a, b$
$a$
$b(t) = 1 - e^{-\frac{t}{R_p C_{load}}}$
$b$
$t$


$R_p$
$a$
$R_n$
$b$
$C_{load}$


$a, b$
$a$
$b$
$t$
$b(t) = 1 - e^{-\frac{t}{R_p C_{load}}}$
$b(t) = e^{-\frac{t}{R_n C_{load}}}$

# Why this way?



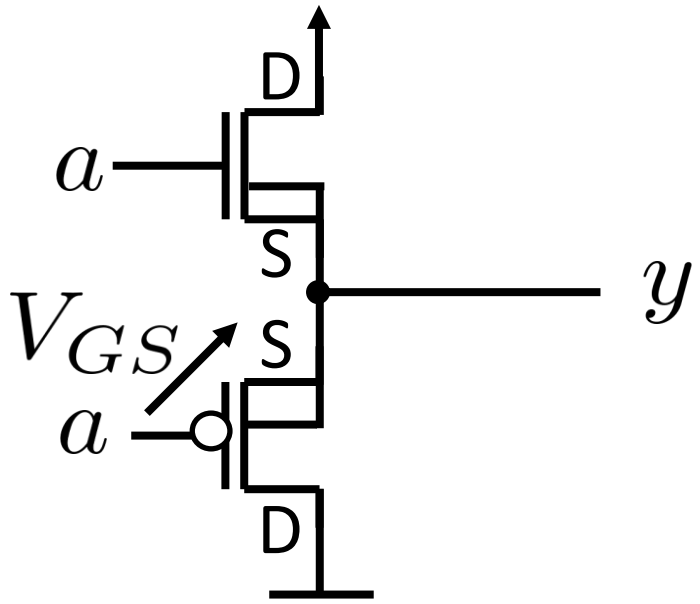

$V_{GS}$ independent of $y$

-> high a -> nMOS always connects

-> pulls down y to 0V (= strong 0)

# pMOS pulling down

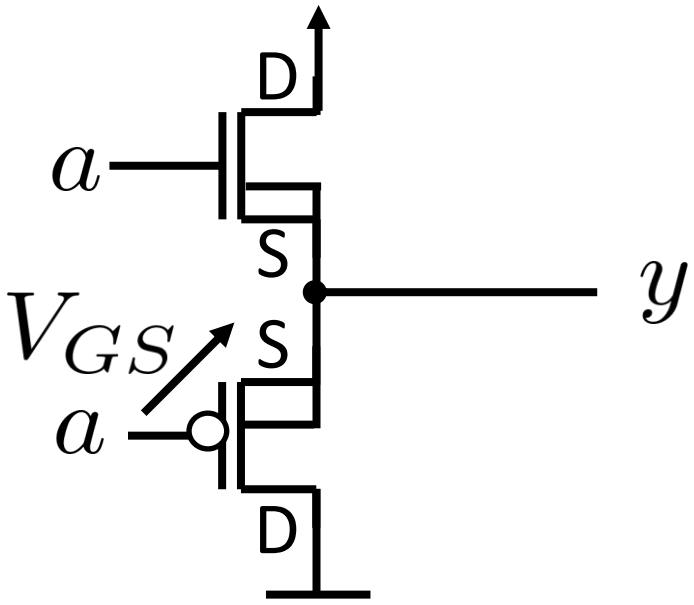
... not inverter,
but also:

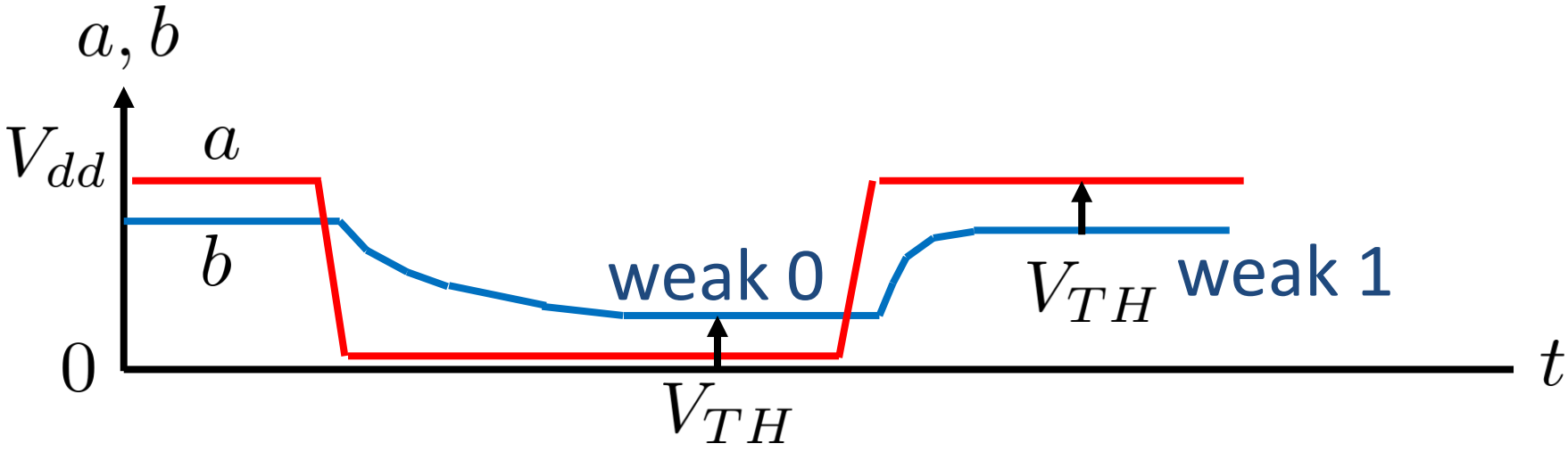



$V_{GS}$ depends on $y$

-> when $y \leq V_{TH}$ : pMOS cutoff

-> pulls down y to $V_{TH}$ (= weak 0)


D
a
S
y
$V_{GS}$
S
a
D


a, b
$V_{dd}$
a
b
0
weak 0
$V_{TH}$
$V_{TH}$
weak 1
t

# CMOS

nMOS:

drives strong 0, weak 1

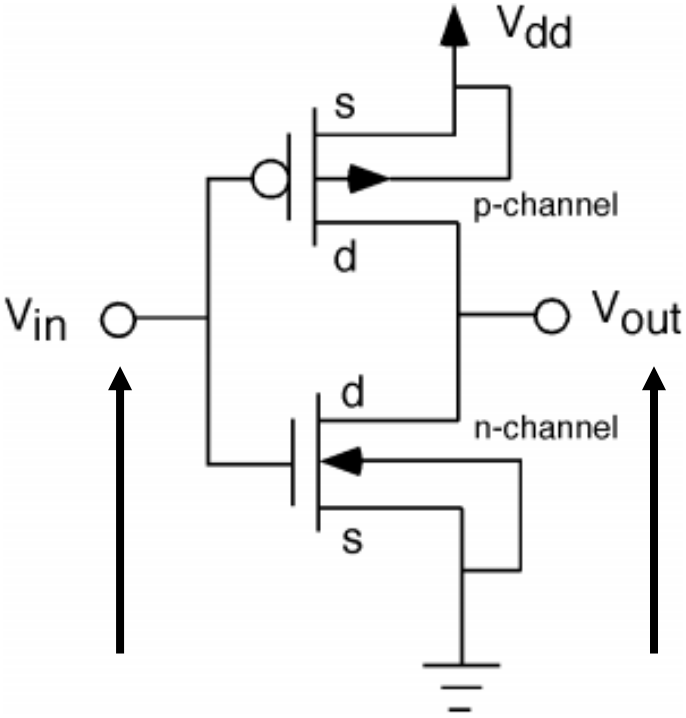
-> used for pull-down

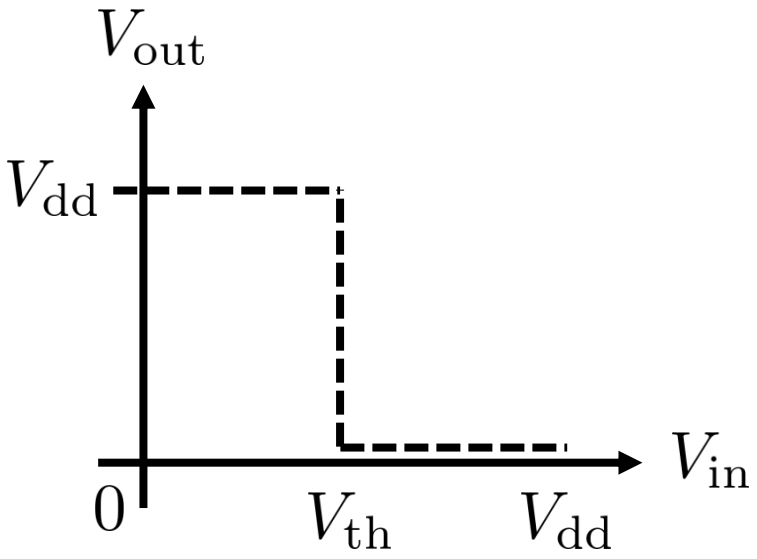
pMOS:

drives strong 1, weak 0

-> used for pull-up

# CMOS Inverter – switch model

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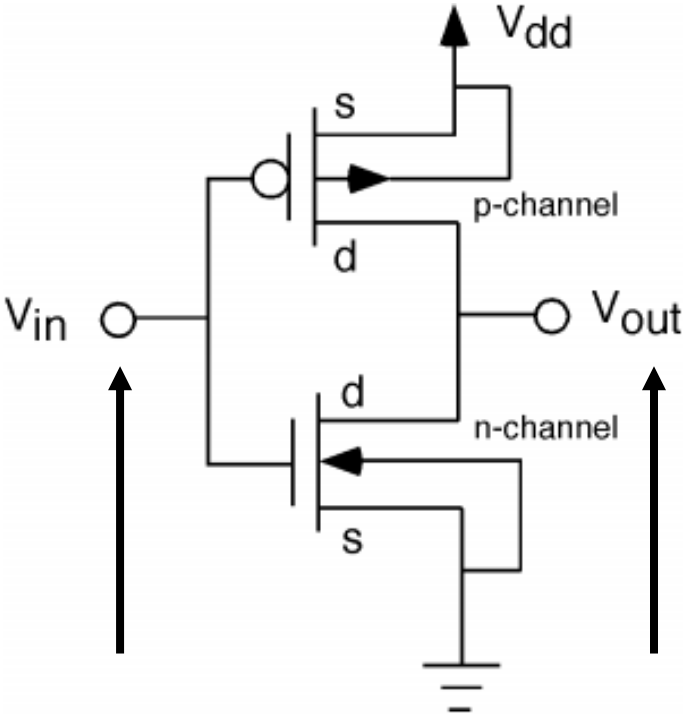
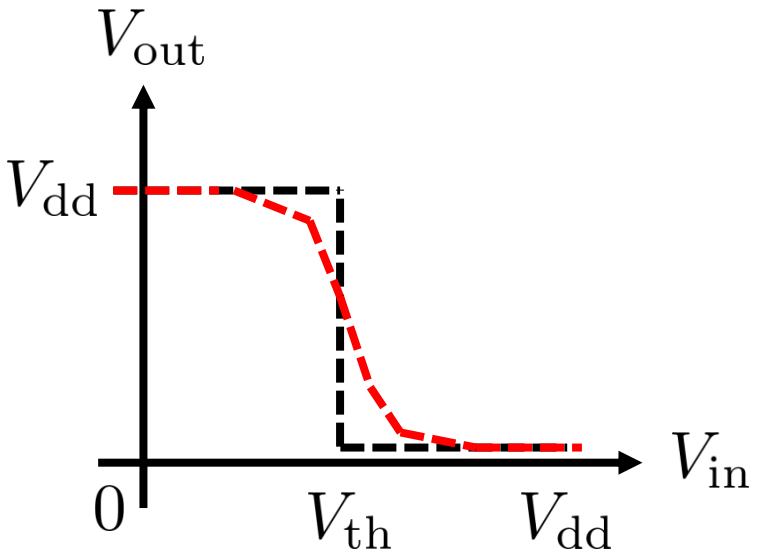
# CMOS Inverter – detailed static

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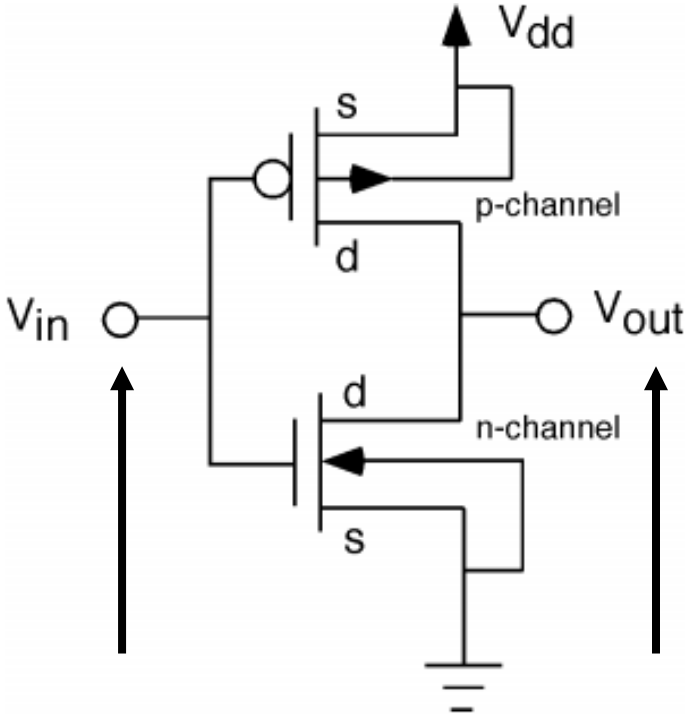
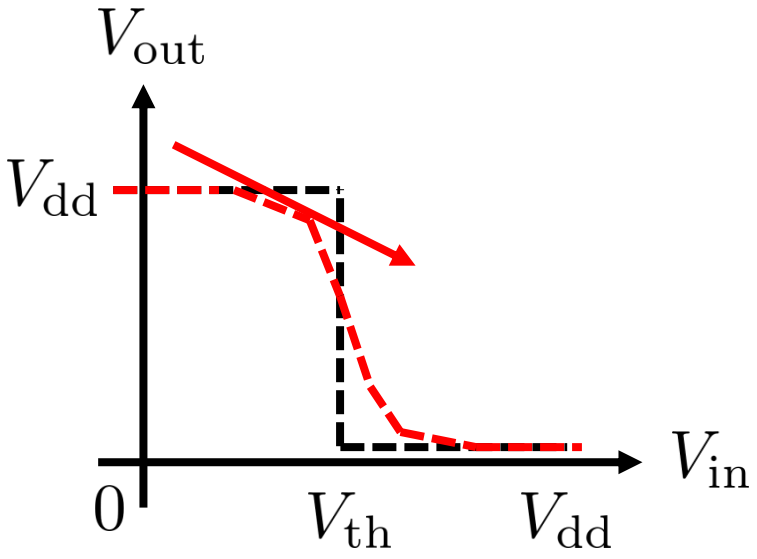
# CMOS Inverter – gain




$$g(x) = \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=x}$$

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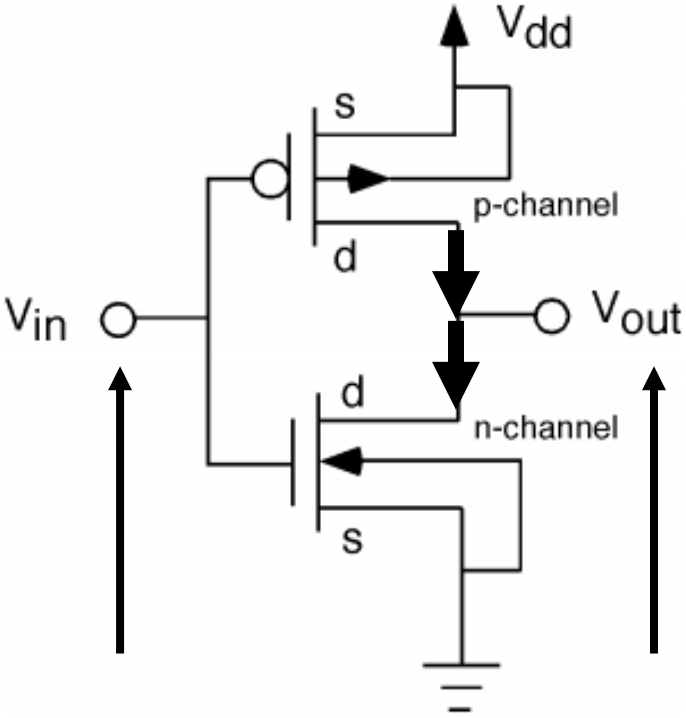
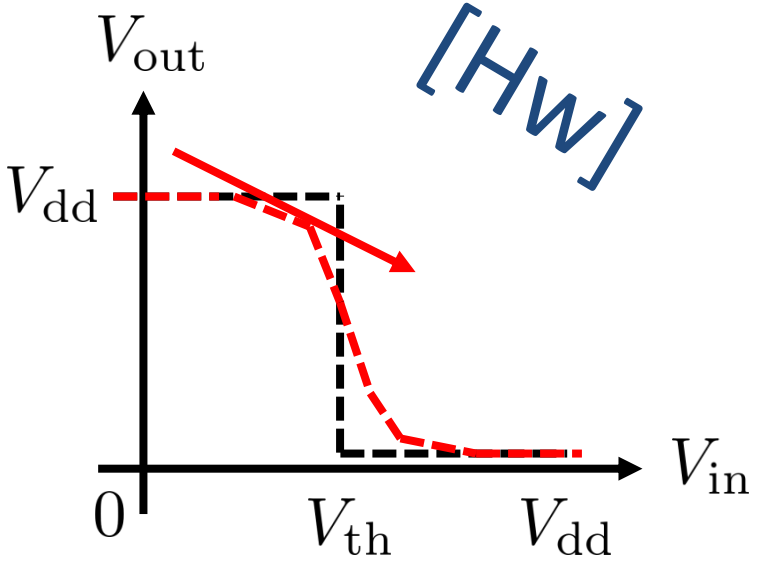
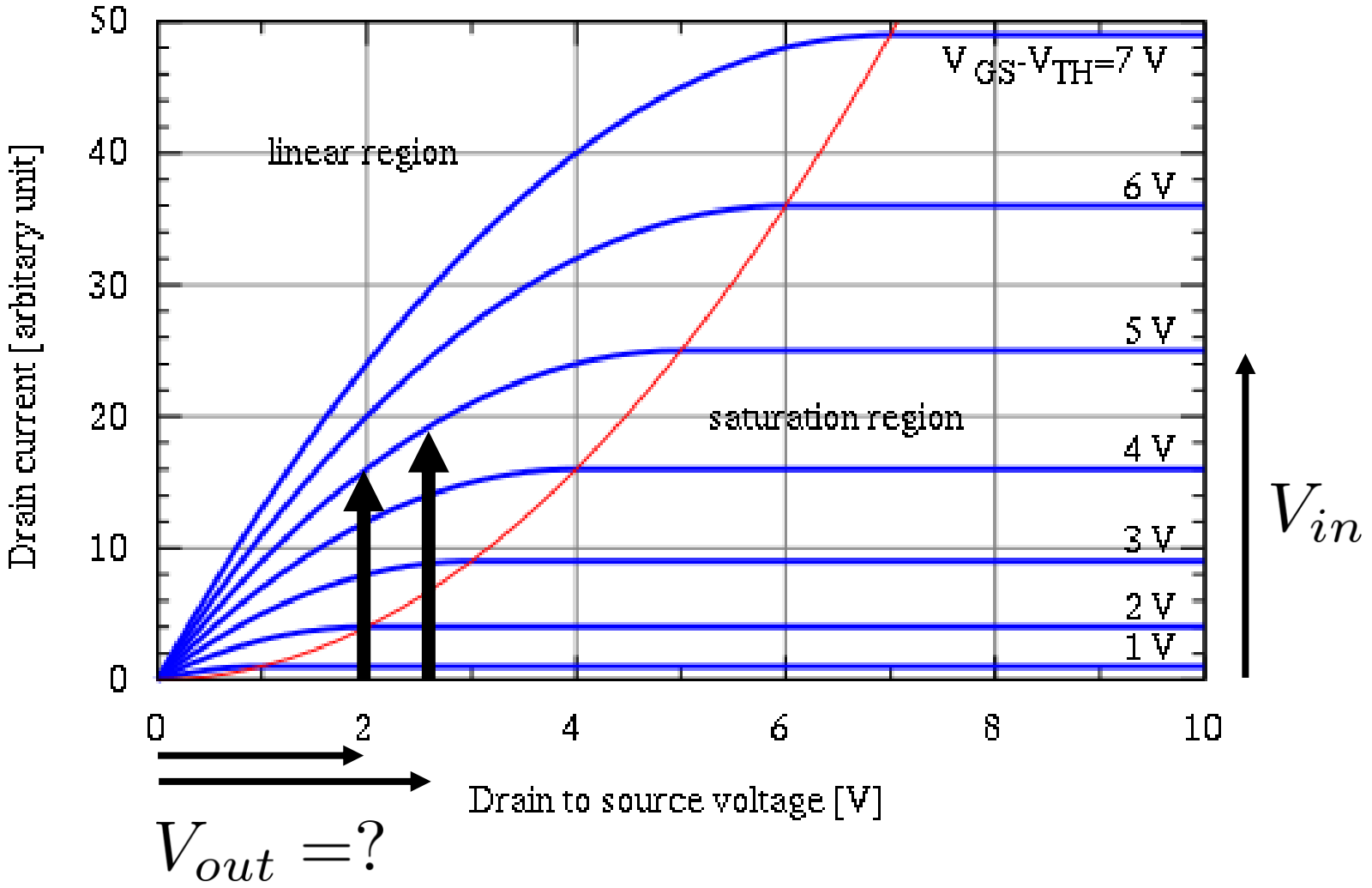
# CMOS Inverter – detailed static




[HW]

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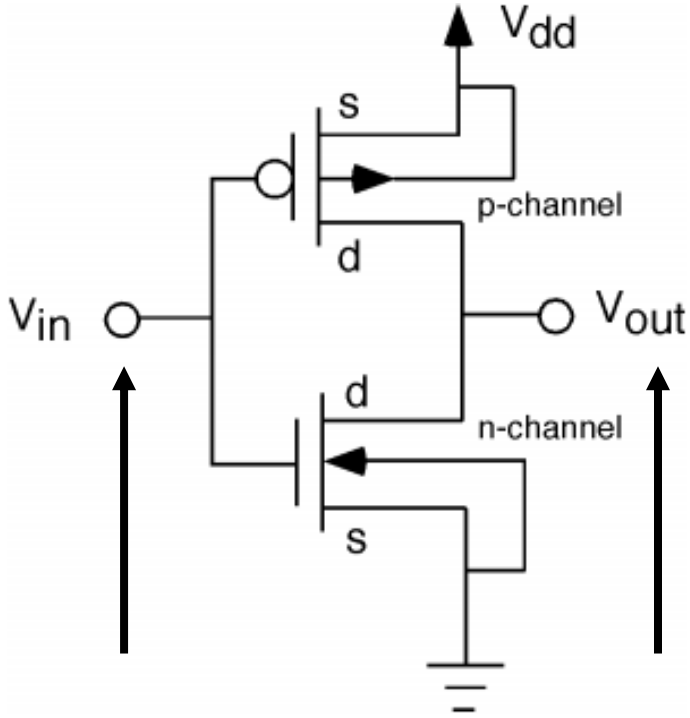
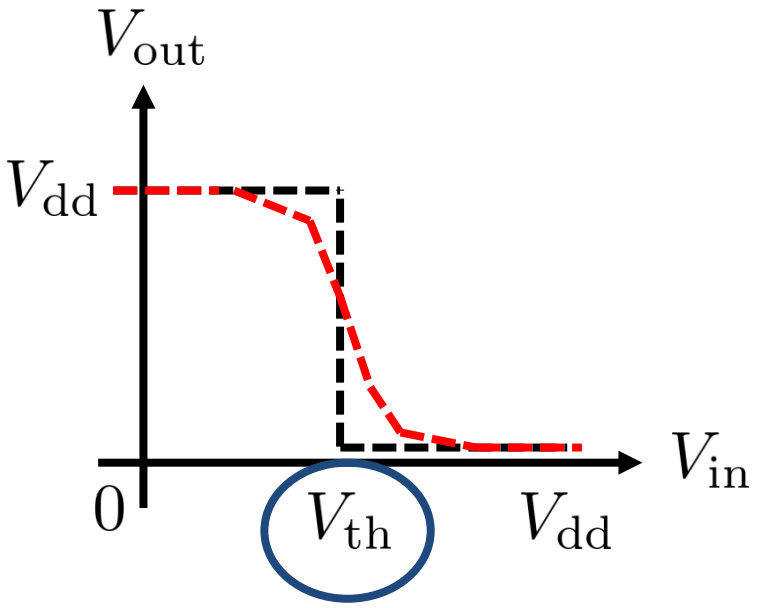



Threshold can be moved by relative sizing

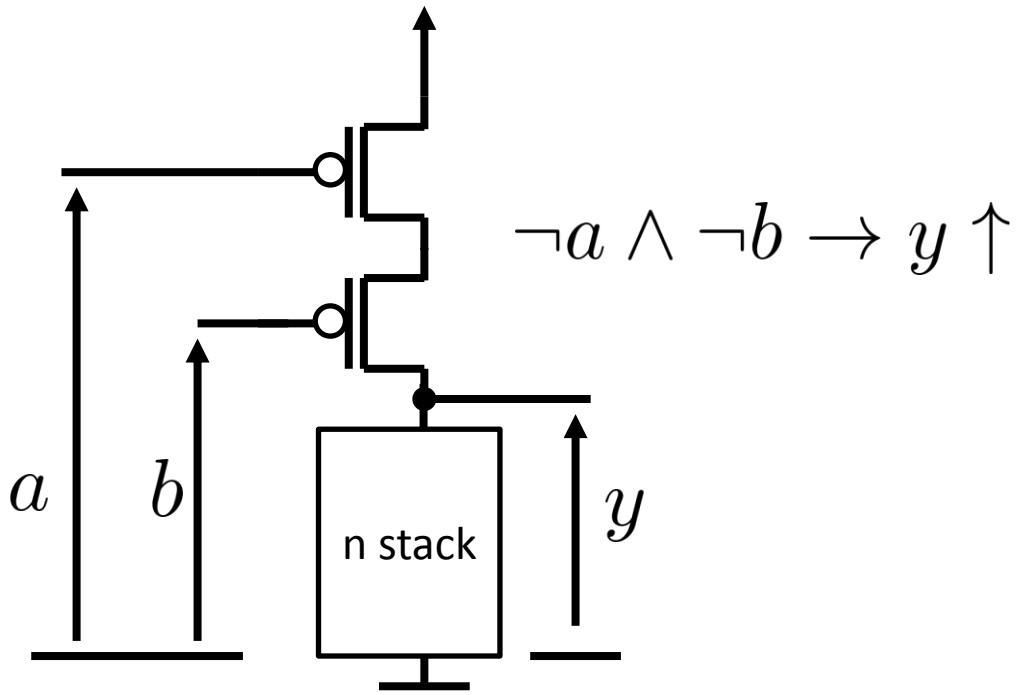
-> low/high-threshold INV

# CMOS Design

Combinational Logic:

n-stack: down transition $G \rightarrow y\downarrow$

p-stack: up transition $\neg G \rightarrow y\uparrow$

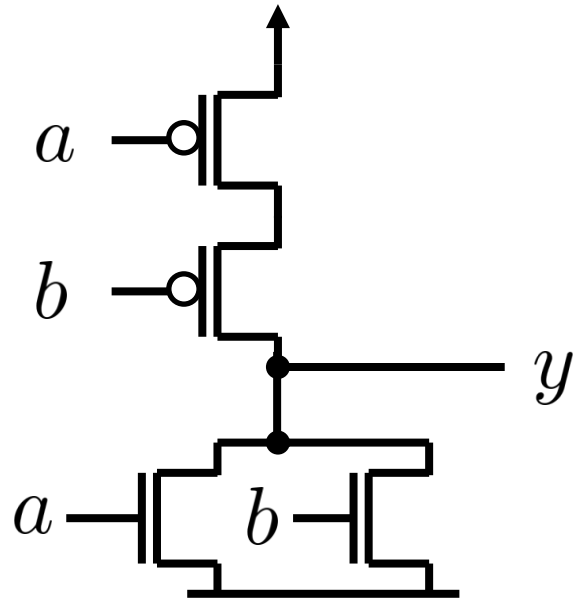


# NOR

Combinational Logic:

n-stack: down transition $a \vee b \rightarrow y \downarrow$

p-stack: up transition $\neg(a \vee b) \rightarrow y \uparrow$



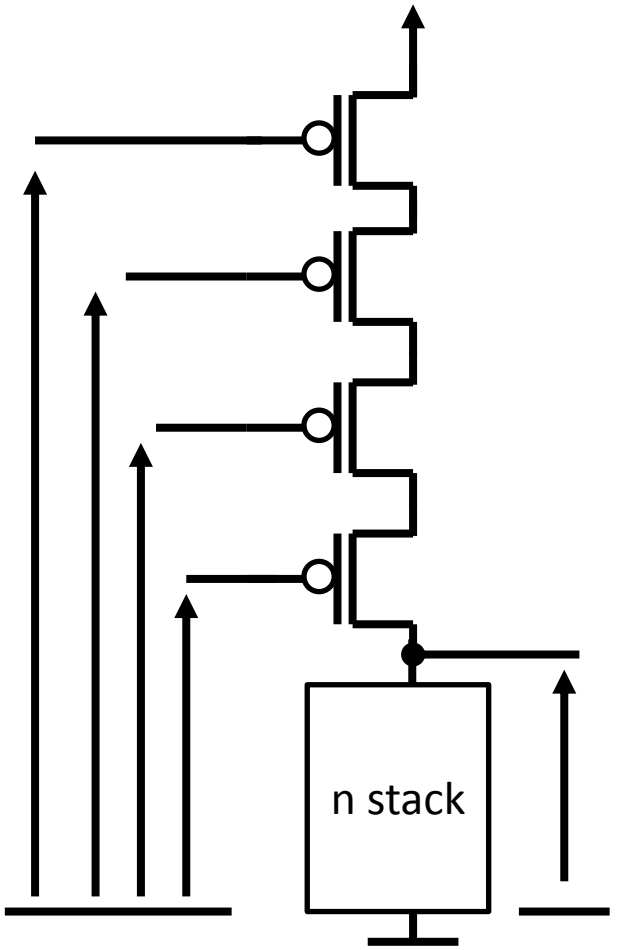
# CMOS Design

Deep stacks slow!

esp. mind deep p-stacks

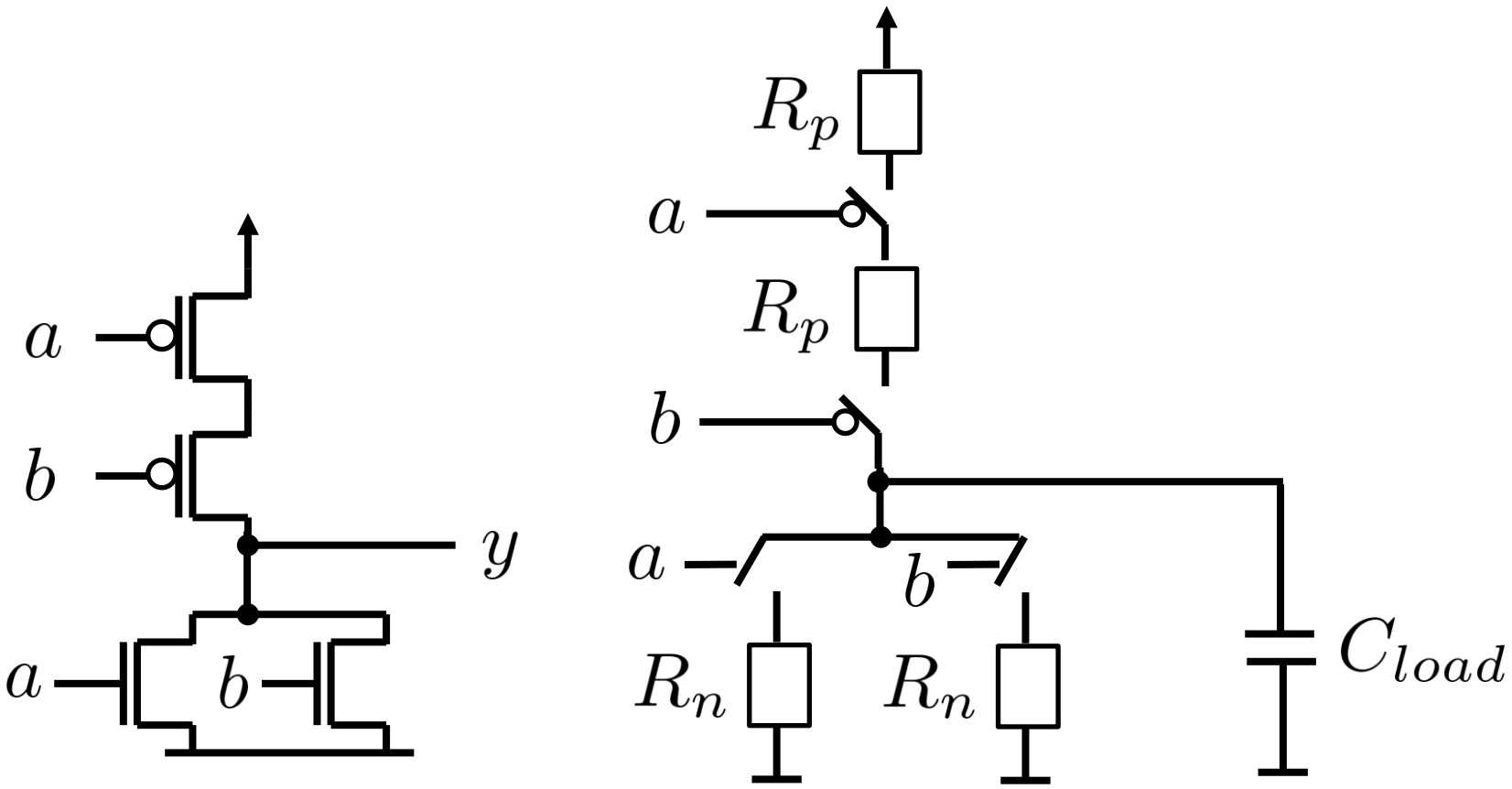
Reason: remember

resistor/switch model



# CMOS Design

We want NOR to be as fast as INV.

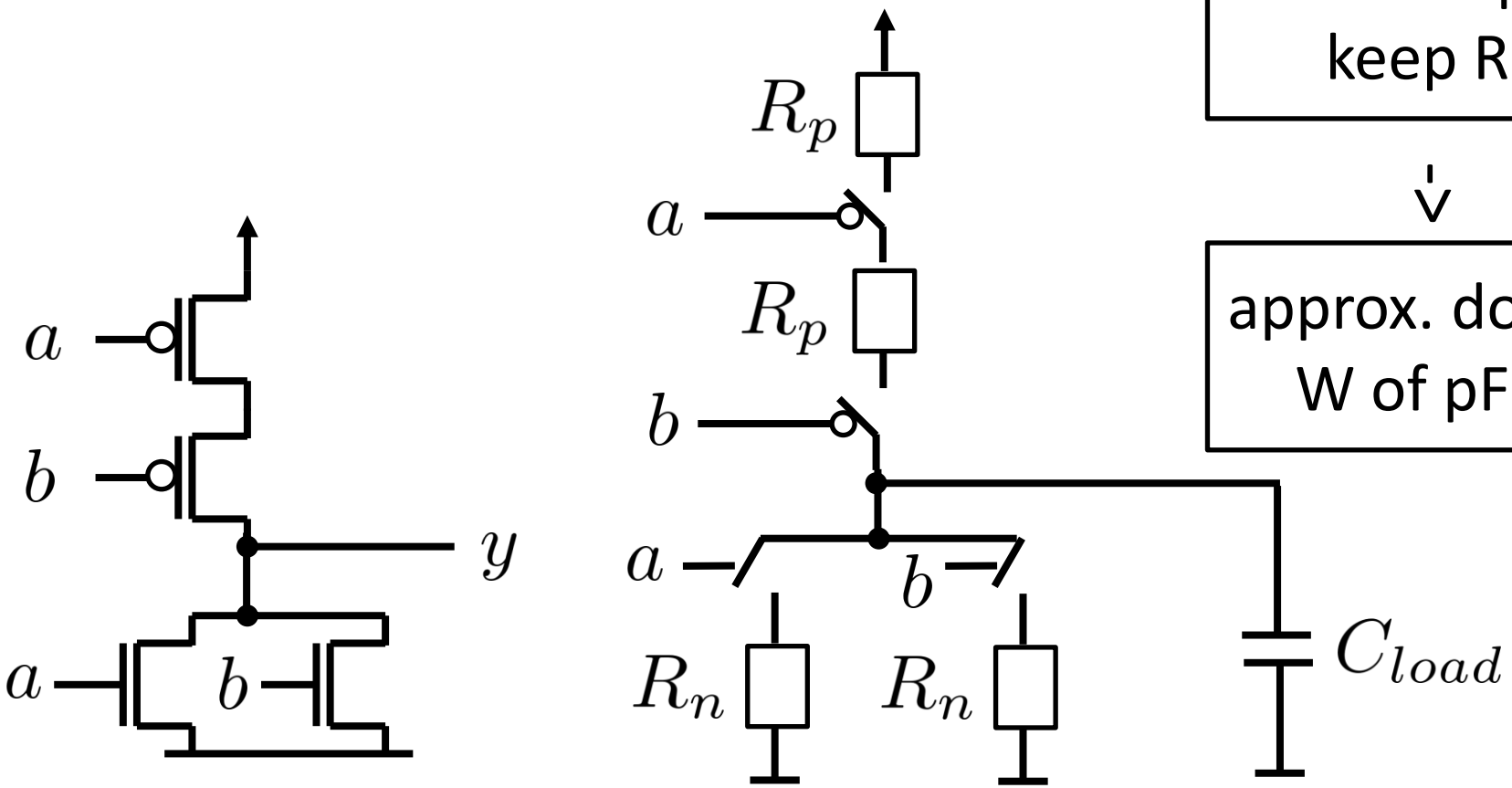


# CMOS Design

We want NOR to be as fast as INV ->

half Rp
keep Rn

approx. double
W of pFET



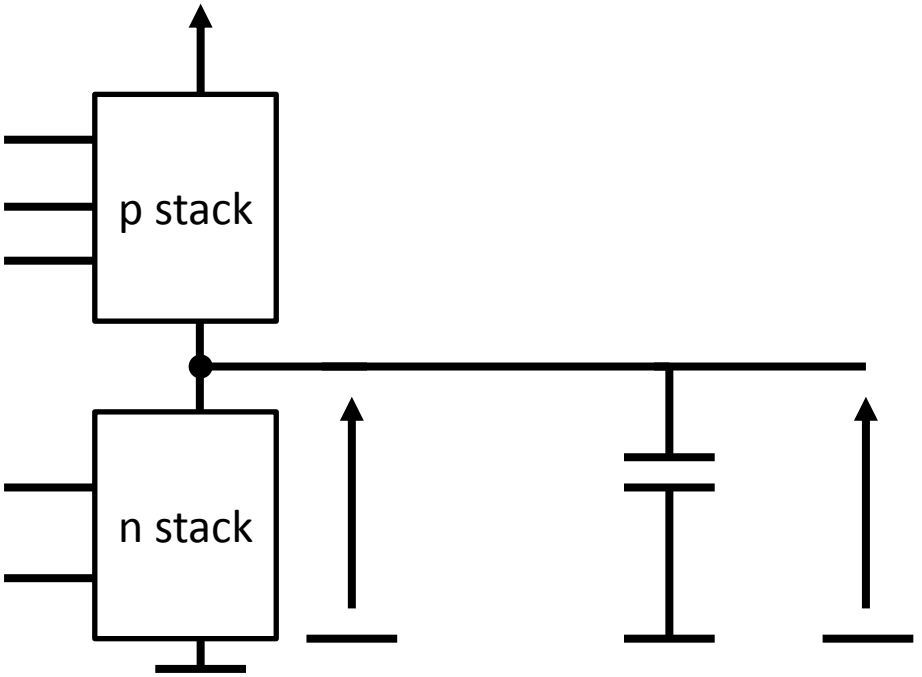
# State holding logic?

$$G_{\mathrm{down}} \rightarrow y \downarrow$$
$$G_{\mathrm{up}} \rightarrow y \uparrow$$

-> statesizer!

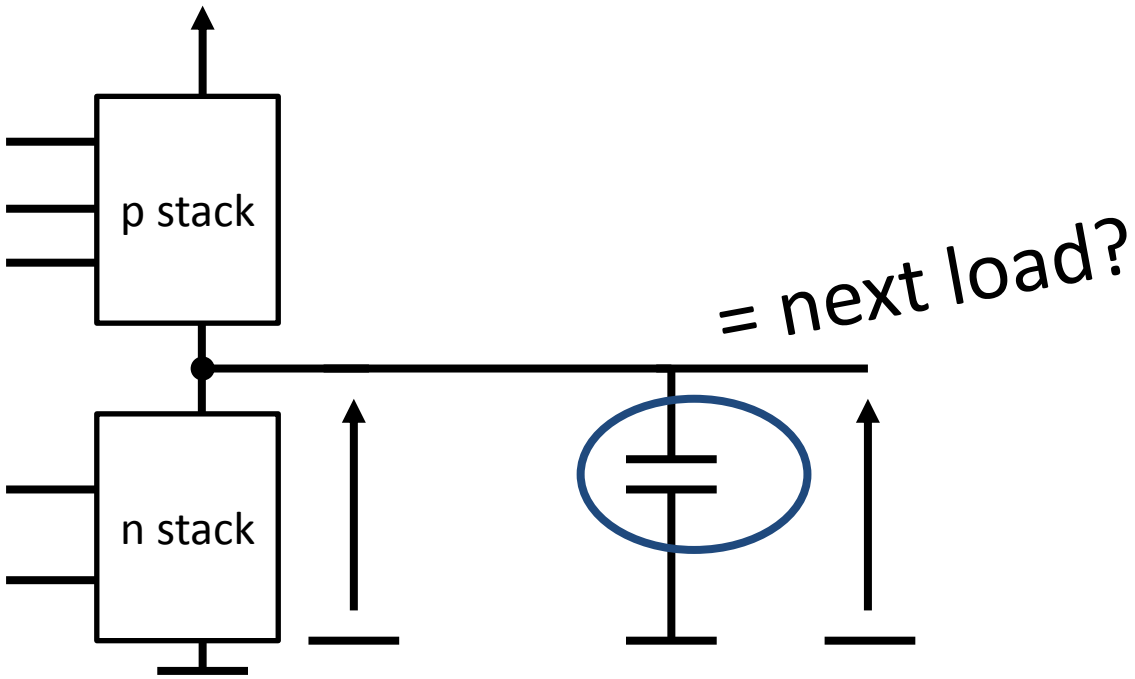
# V1 - State holding logic

$$G_{\text{down}} \rightarrow y \downarrow$$
$$G_{\text{up}} \rightarrow y \uparrow$$



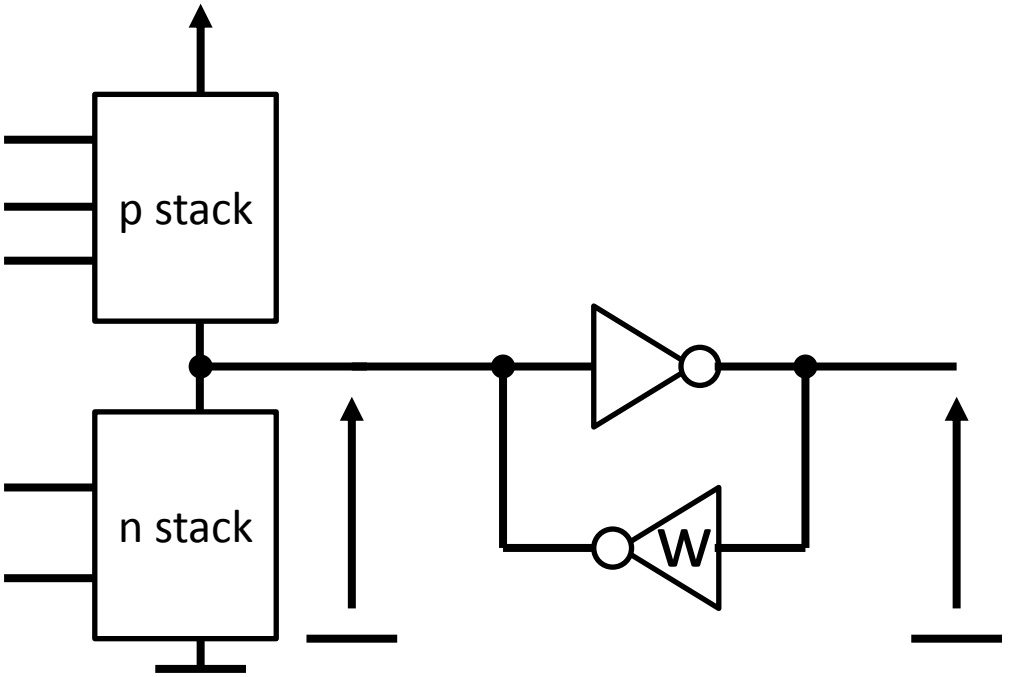
# V1’ - State holding logic

$$G_{\text{down}} \rightarrow y \downarrow$$
$$G_{\text{up}} \rightarrow y \uparrow$$



# V2 - State holding logic

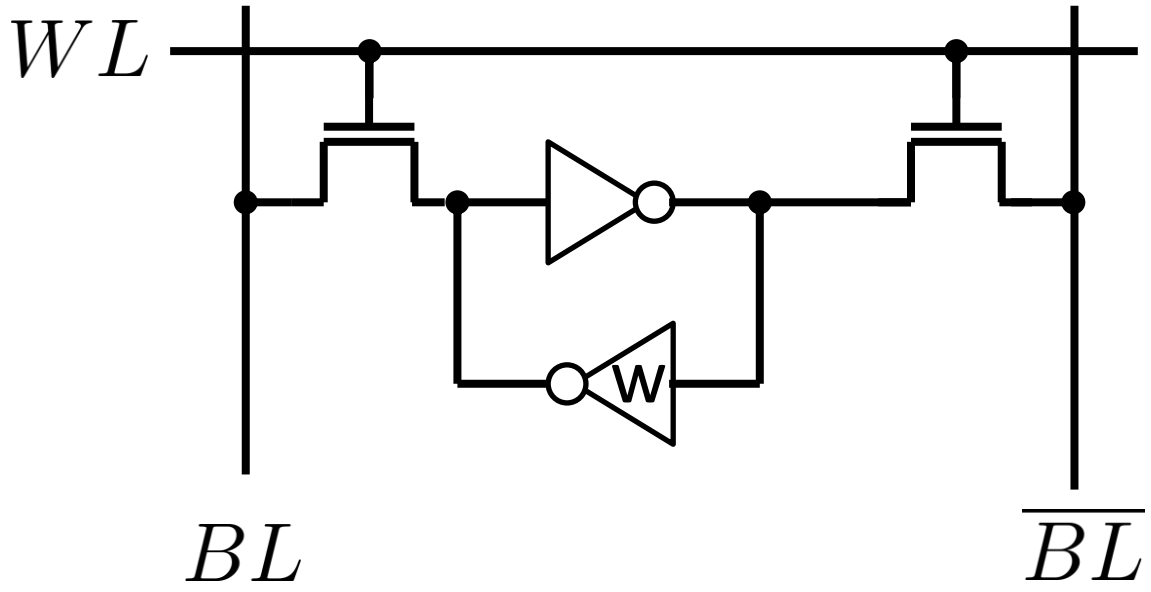
$$G_{\text{down}} \rightarrow y \downarrow$$
$$G_{\text{up}} \rightarrow y \uparrow$$



# State holding logic

Both used in memory design...

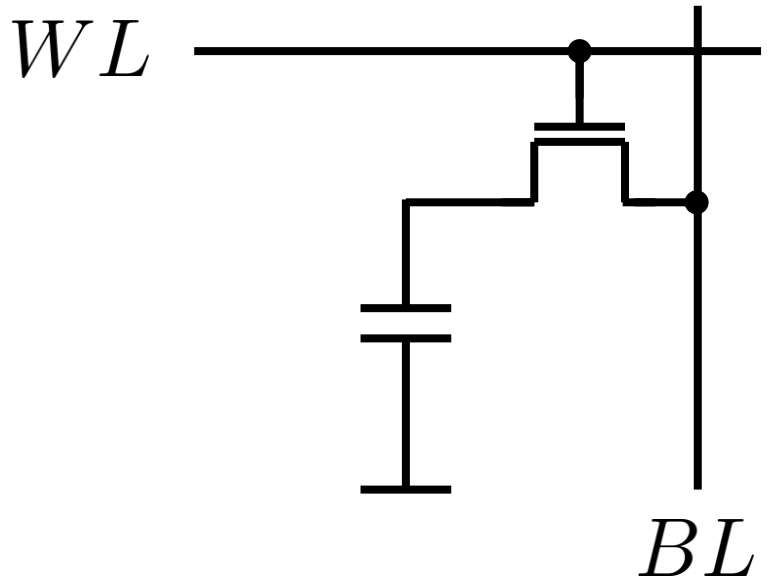
6T-SRAM cell



# State holding logic

Both used in memory design...

DRAM cell (refresh ~ 20Hz)



# V3 - State holding logic *[Hw]*

$$\begin{aligned} G_{\text{down}} &\rightarrow y\downarrow \\ G_{\text{up}} &\rightarrow y\uparrow \end{aligned}$$

->

$$\begin{aligned} G_{\text{down}} \vee (\neg y \wedge \neg G_{\text{up}}) &\rightarrow y\downarrow \\ G_{\text{up}} \vee (y \wedge \neg G_{\text{down}}) &\rightarrow y\uparrow \end{aligned}$$

->

$$\begin{aligned} G_{\text{down}} \vee (\neg y \wedge \neg G_{\text{up}}) &\rightarrow y'\downarrow \\ G_{\text{up}} \vee (y \wedge \neg G_{\text{down}}) &\rightarrow y'\uparrow \\ \neg y' &\rightarrow y\downarrow \\ y' &\rightarrow y\uparrow \end{aligned}$$