Beyond classical circuit design lecture 9

Alternative Design Styles

Further Reading

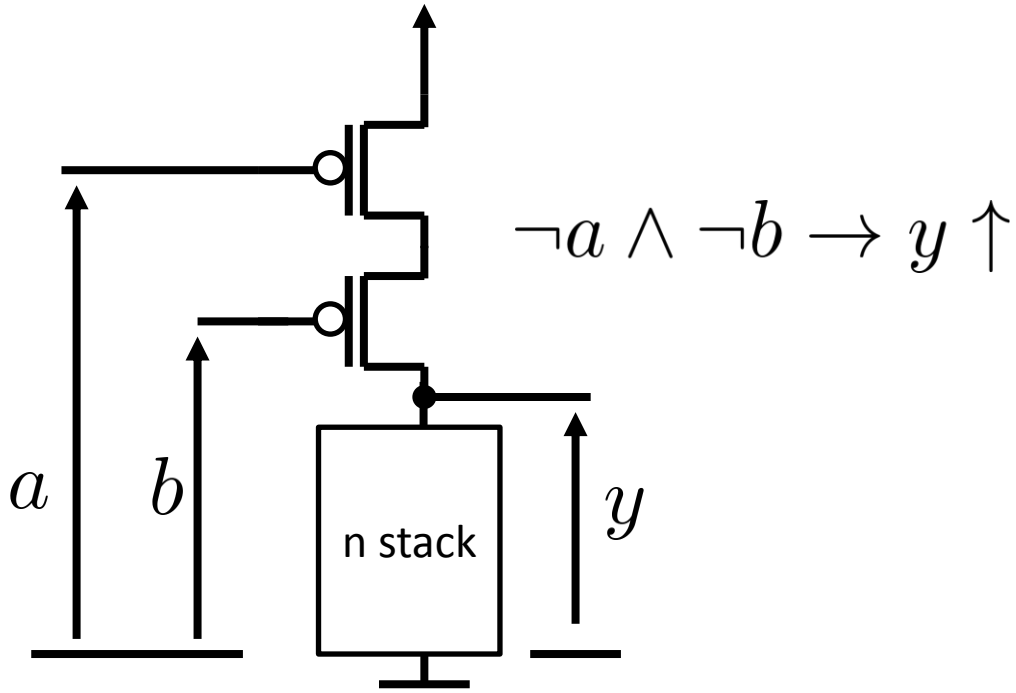
Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic: *Digital Integrated Circuits. A Design Perspective. 2nd edition.* Prentice Hall, 2003.

Remember: CMOS Design

Combinational Logic:

n-stack: down transition $G \rightarrow y\downarrow$

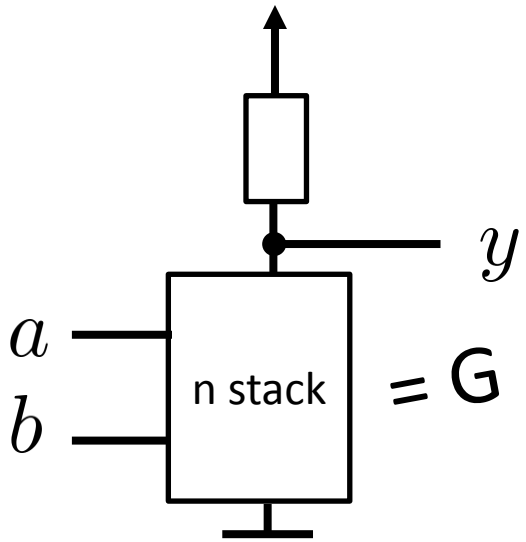
p-stack: up transition $\neg G \rightarrow y\uparrow$



Ratioed-logic: Pull-up

Combinational Logic

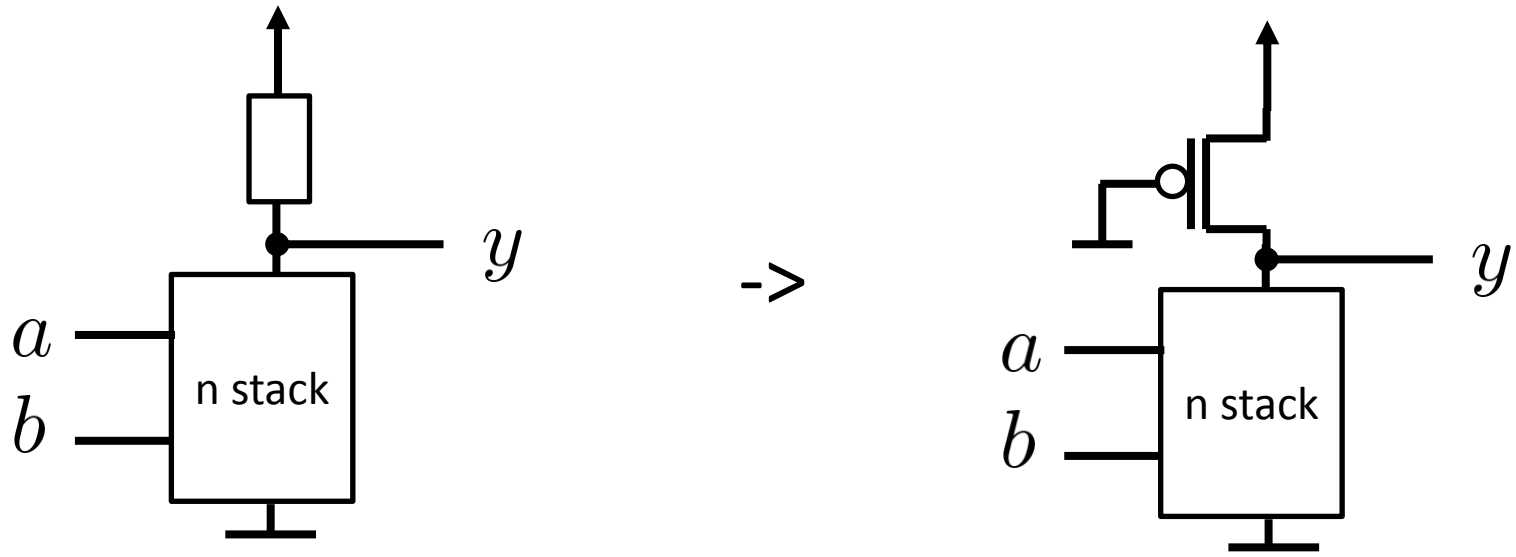
$$G \rightarrow y \downarrow$$
$$\neg G \rightarrow y \uparrow$$



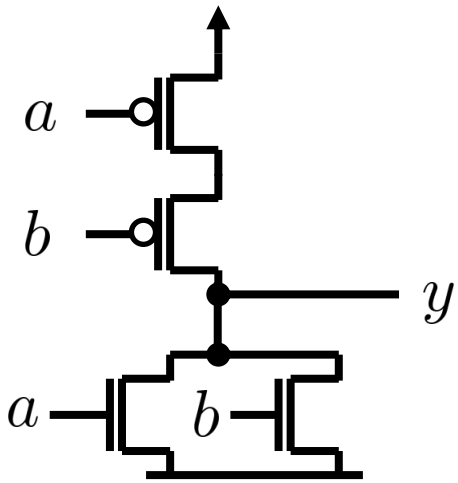
Circuit size?

Static power?

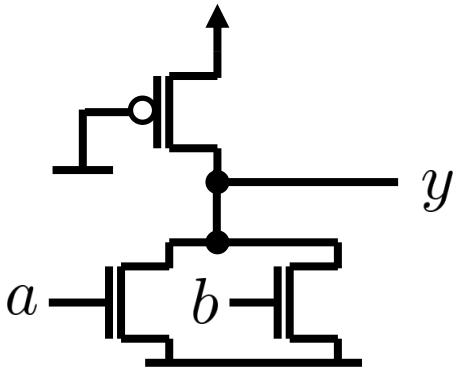
Pseudo-NMOS



Pseudo-NMOS NOR

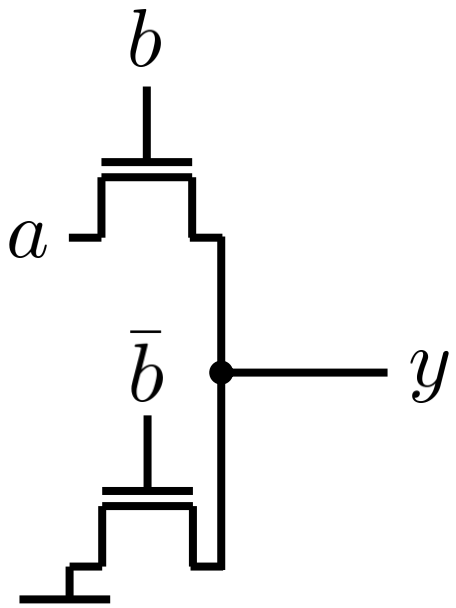


versus



Pass-transistor Logic

AND gate

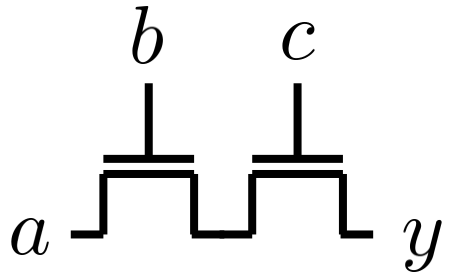


Mind: reduced voltage swing!

Pass-transistor Logic

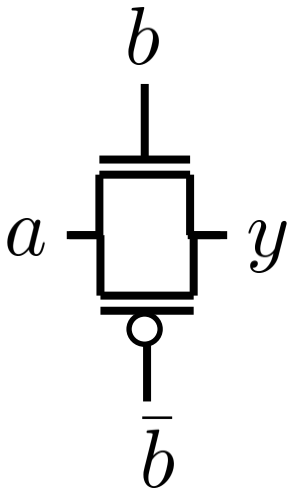
In general:

... what about this wrt. voltage swing?

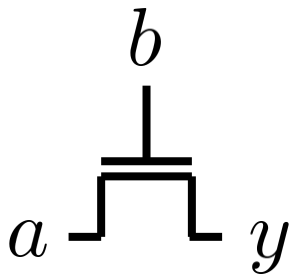


Pass-transistor Logic

Complete pass gate



versus



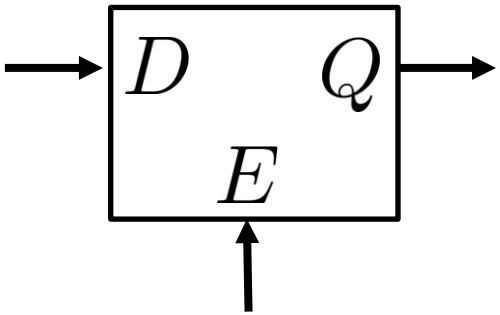
[Hw]

Beyond classical circuit design
lecture 9.5

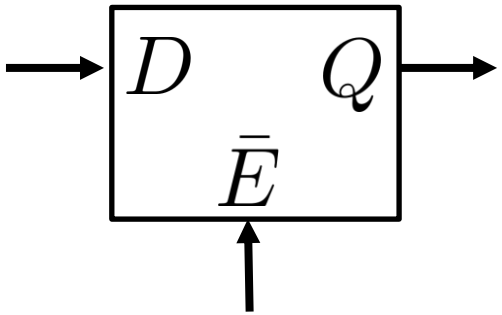
Clocked Design Styles

Latch

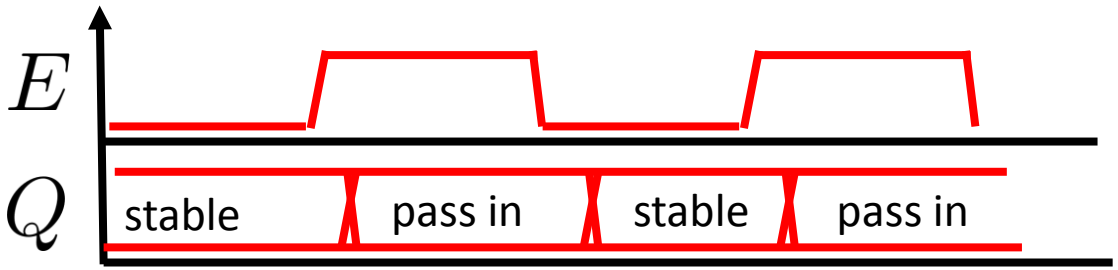
Positive latch



Negative latch

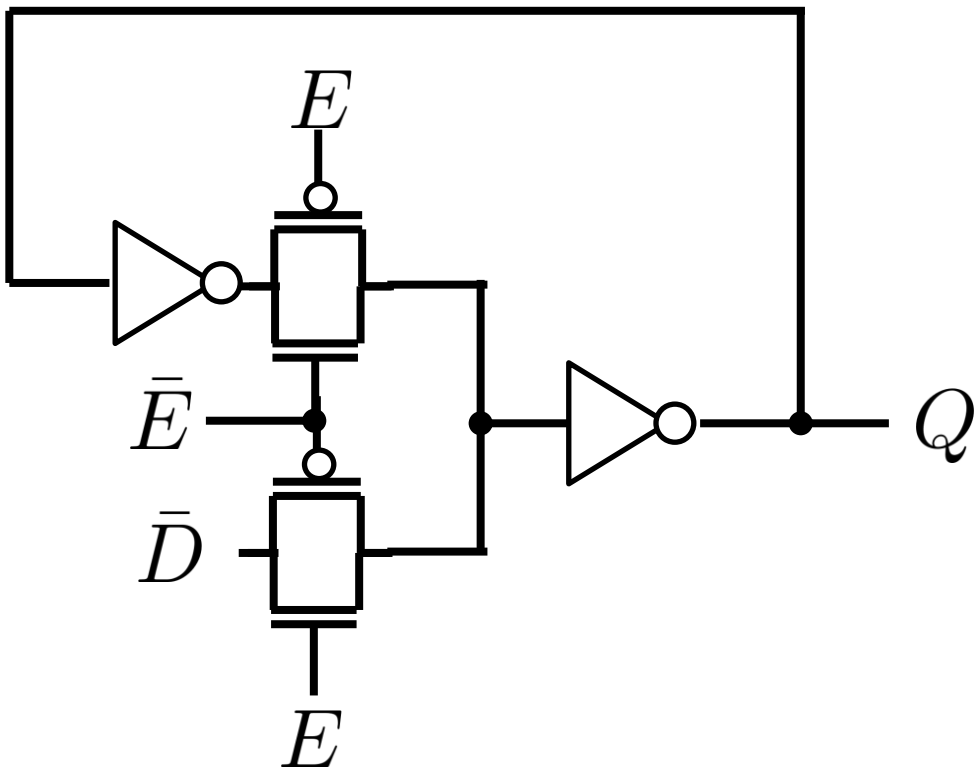


Positive latch behavior



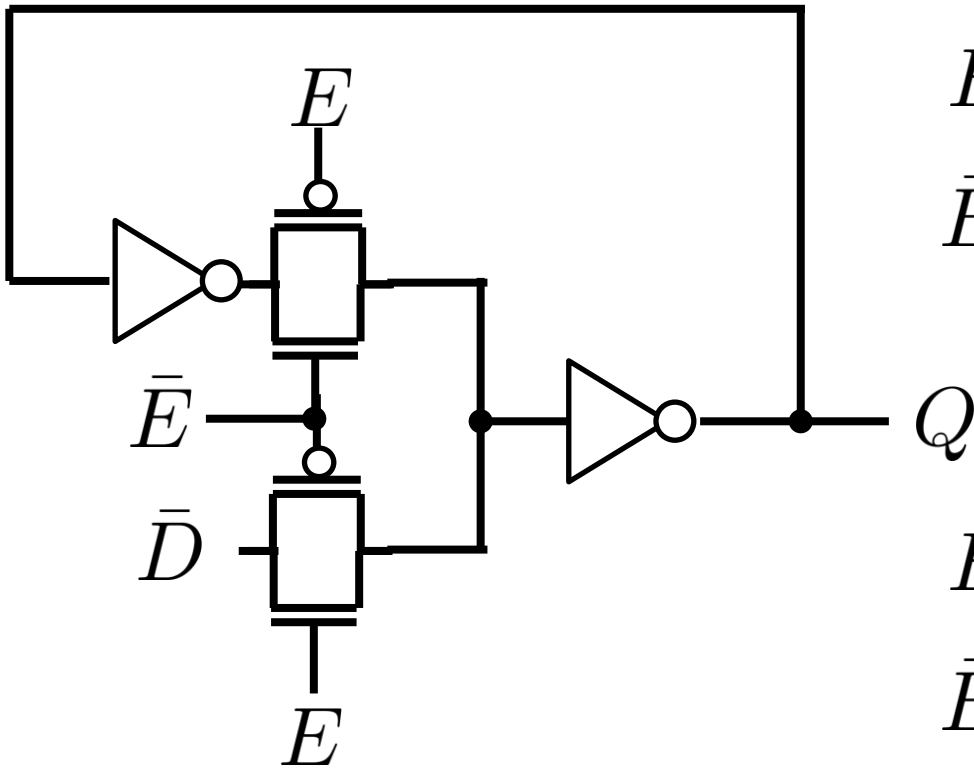
Positive Latch Implementation

by transmission gates

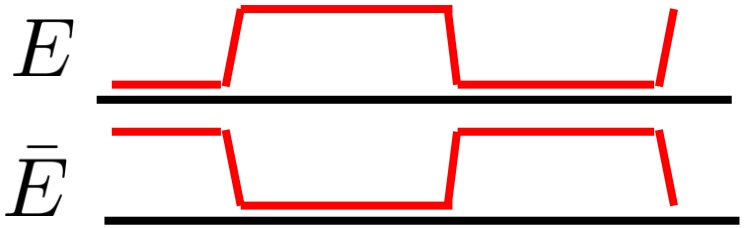


Positive Latch Implementation

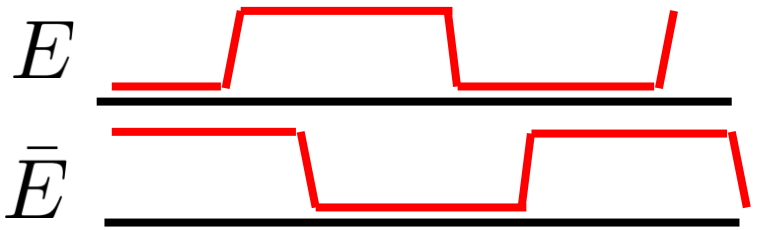
by transmission gates



But mind:

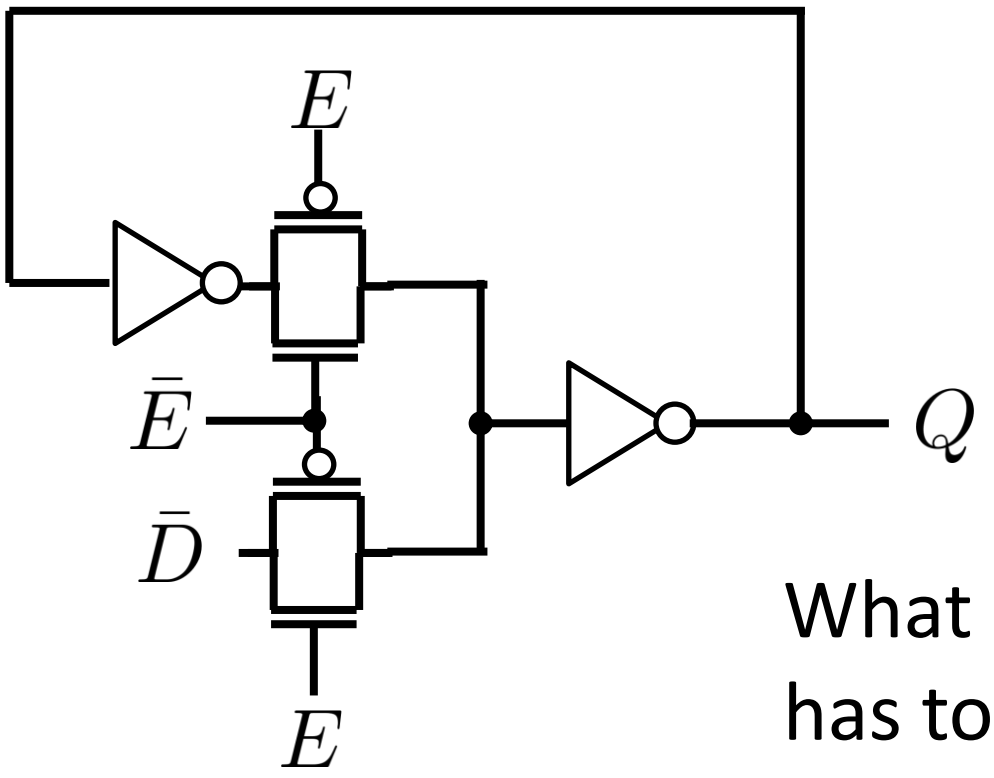


versus



Positive Latch Implementation

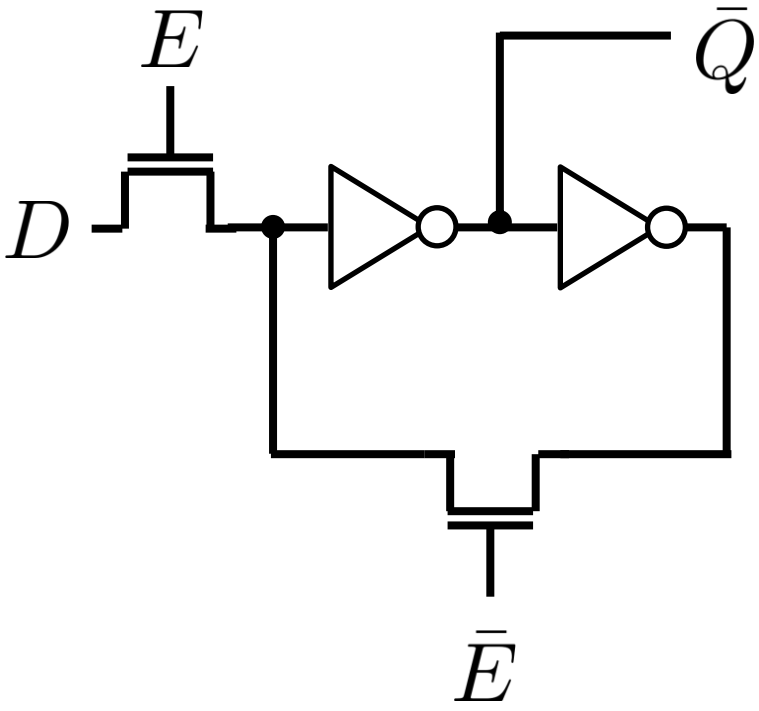
by transmission gates



What is the load signal E has to drive?

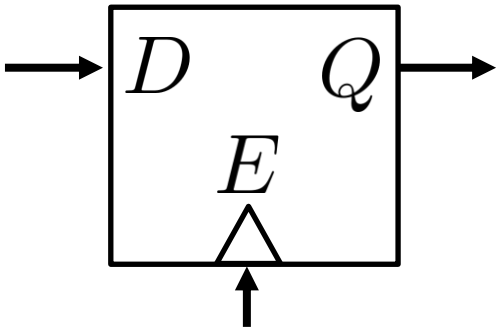
Positive Latch Implementation

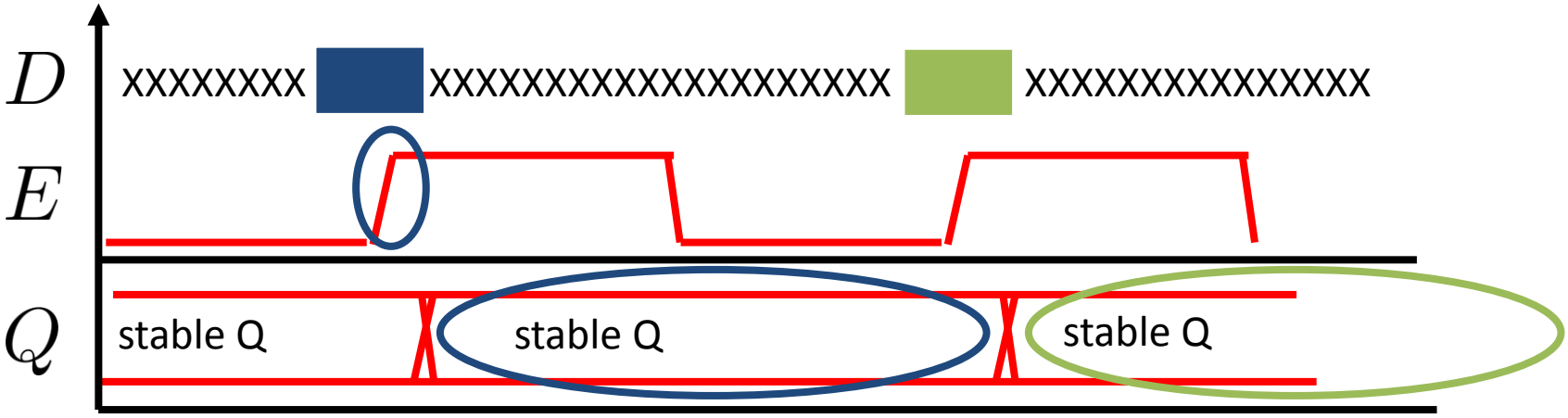
by NMOS pass transistors



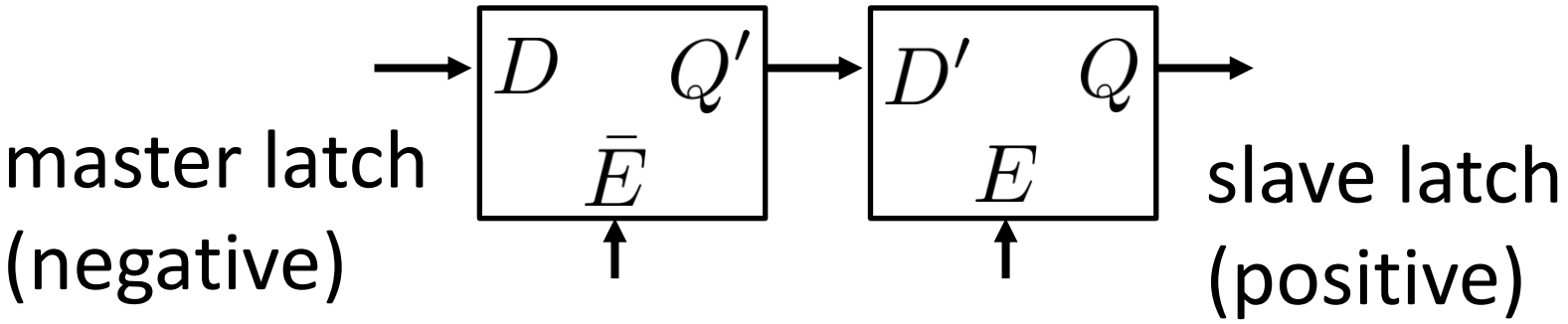
What is the load signal E has to drive?

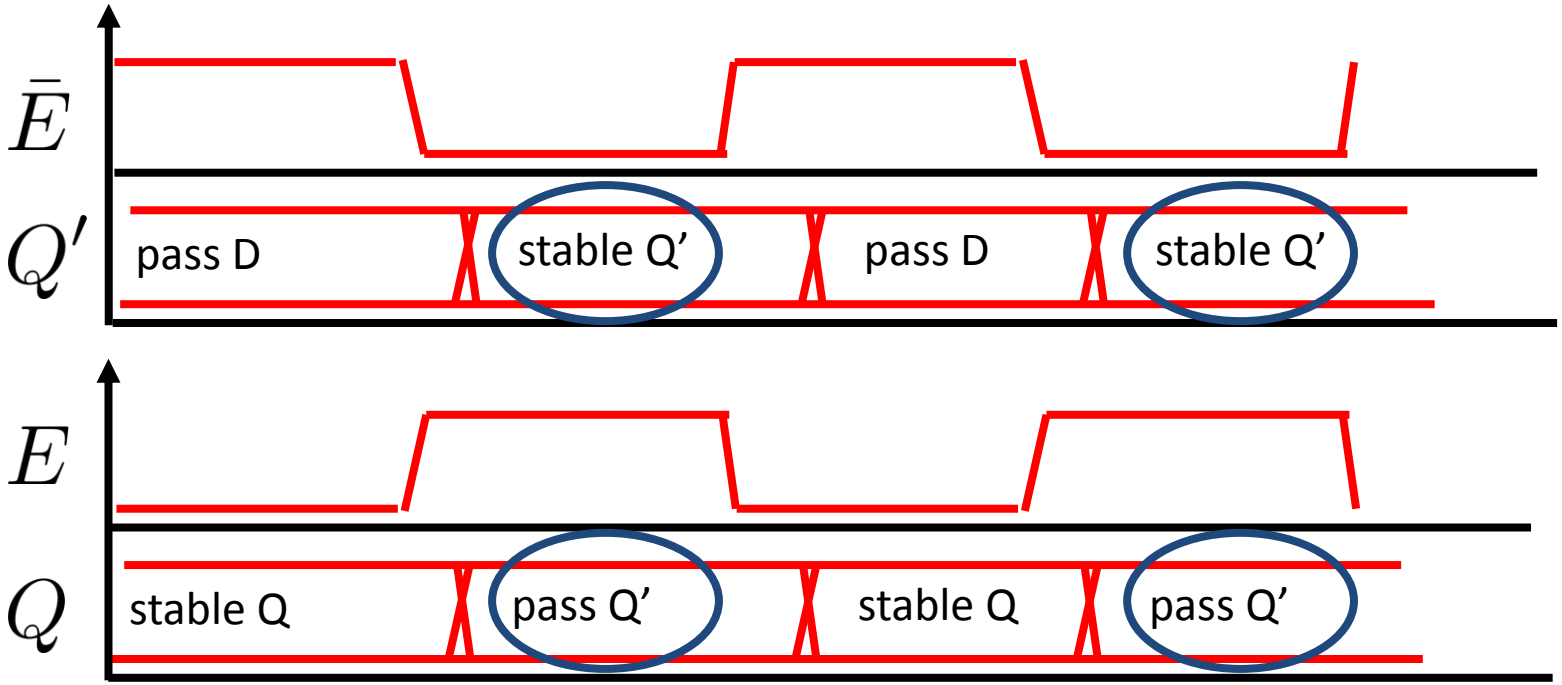
Flip-flop: edge triggered



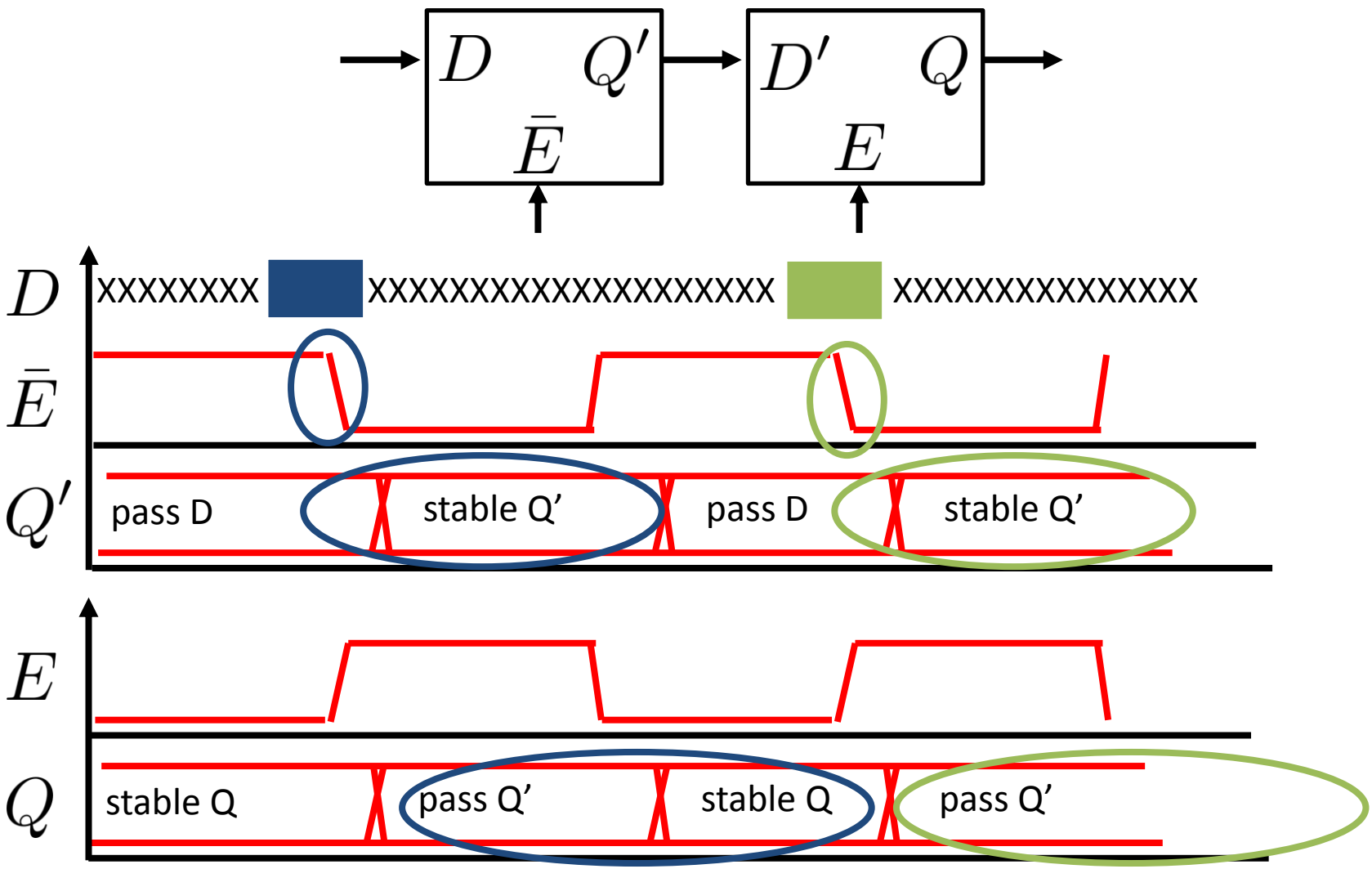


Flip-flop: edge triggered

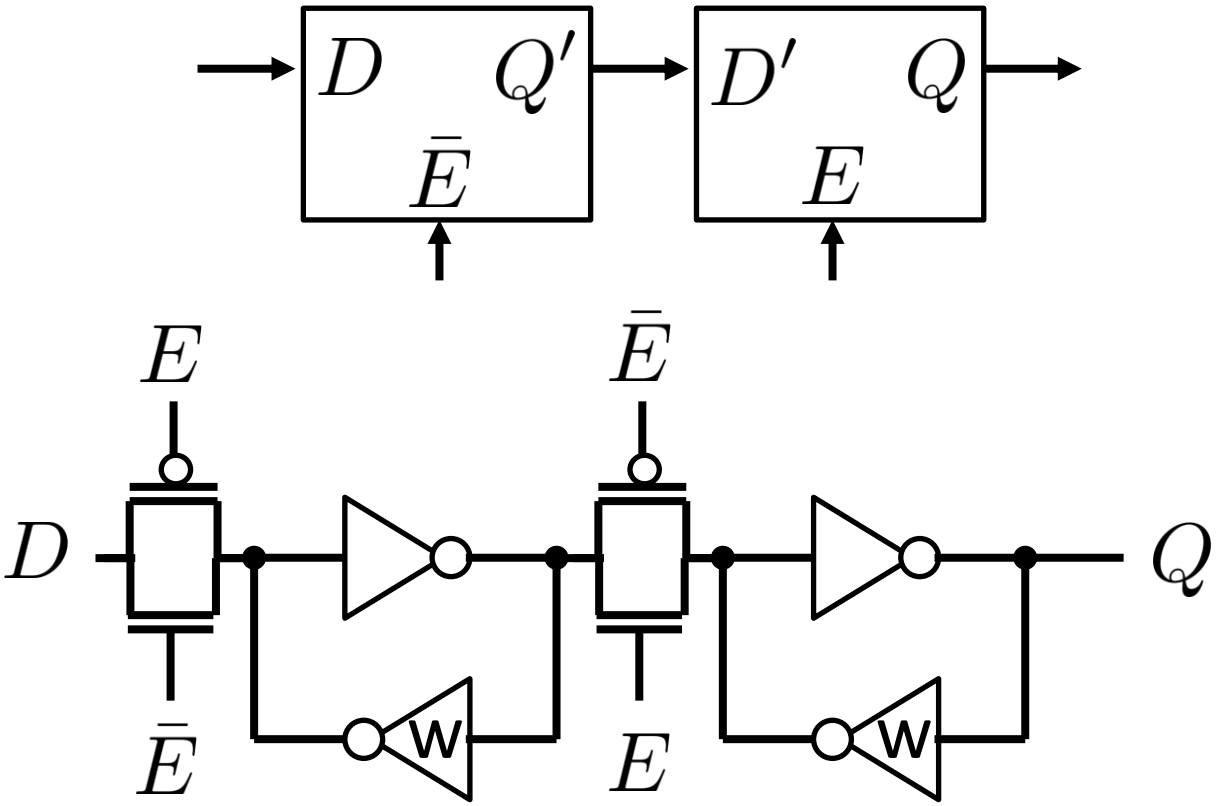




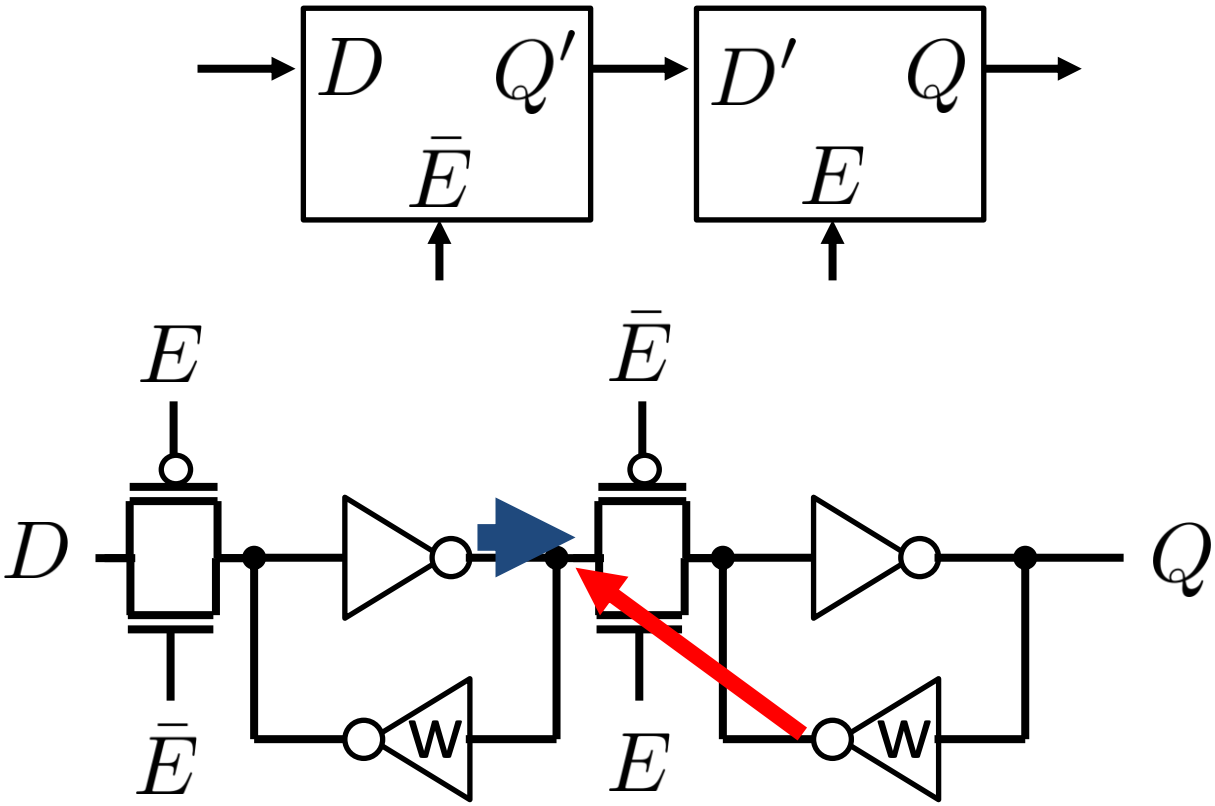
Flip-flop: positive edge triggered



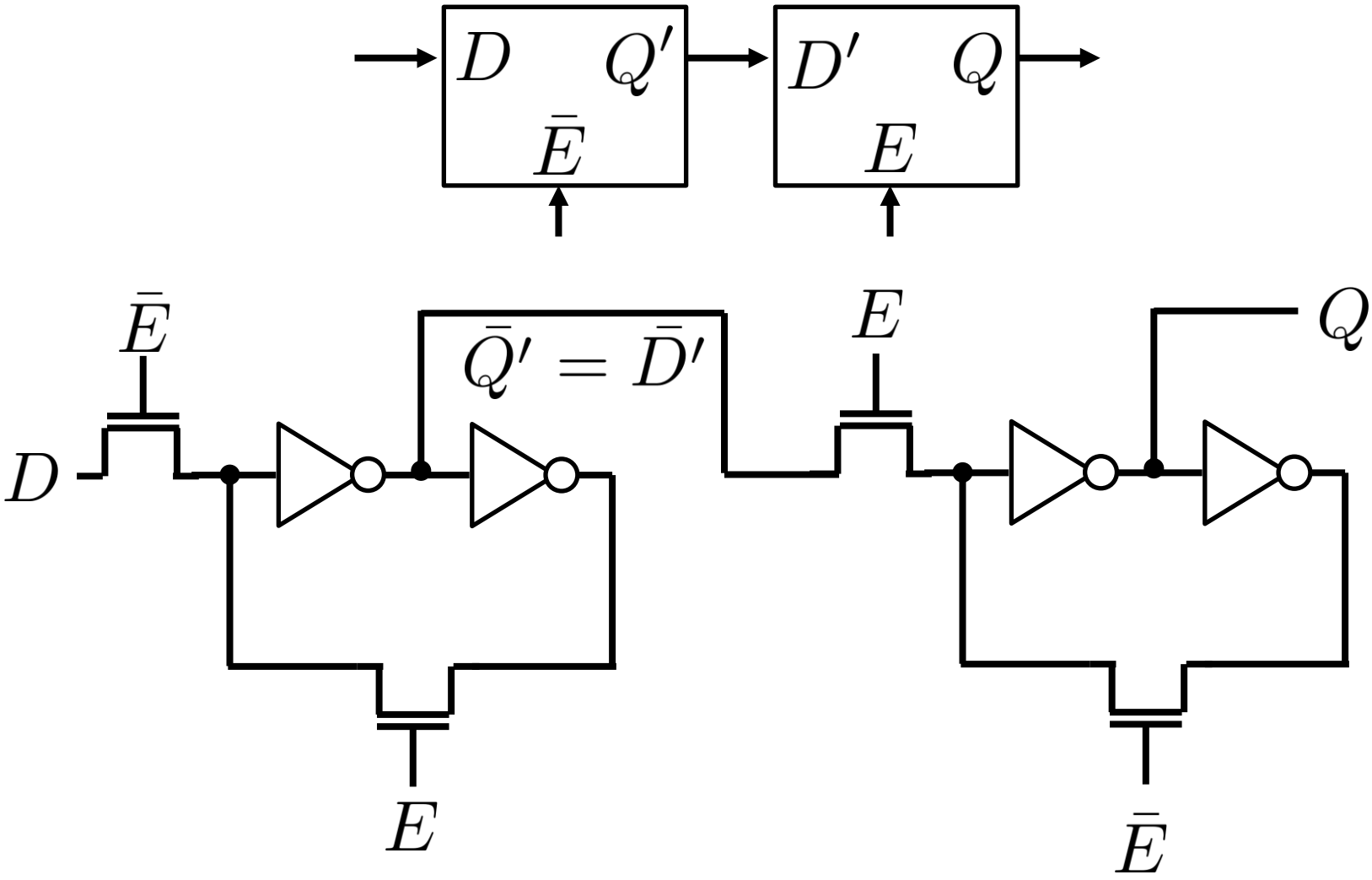
Reducing E-load



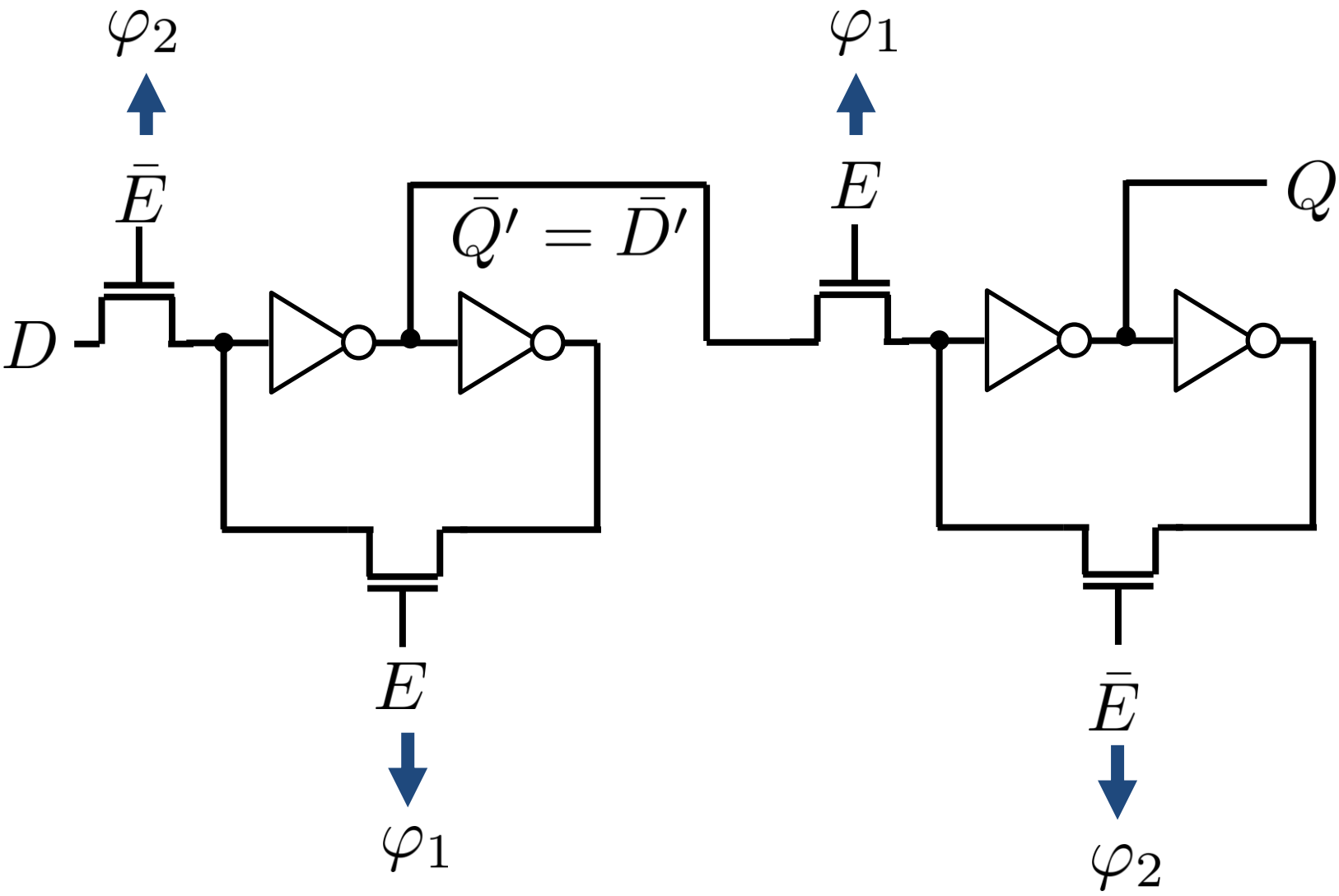
Mind sizing



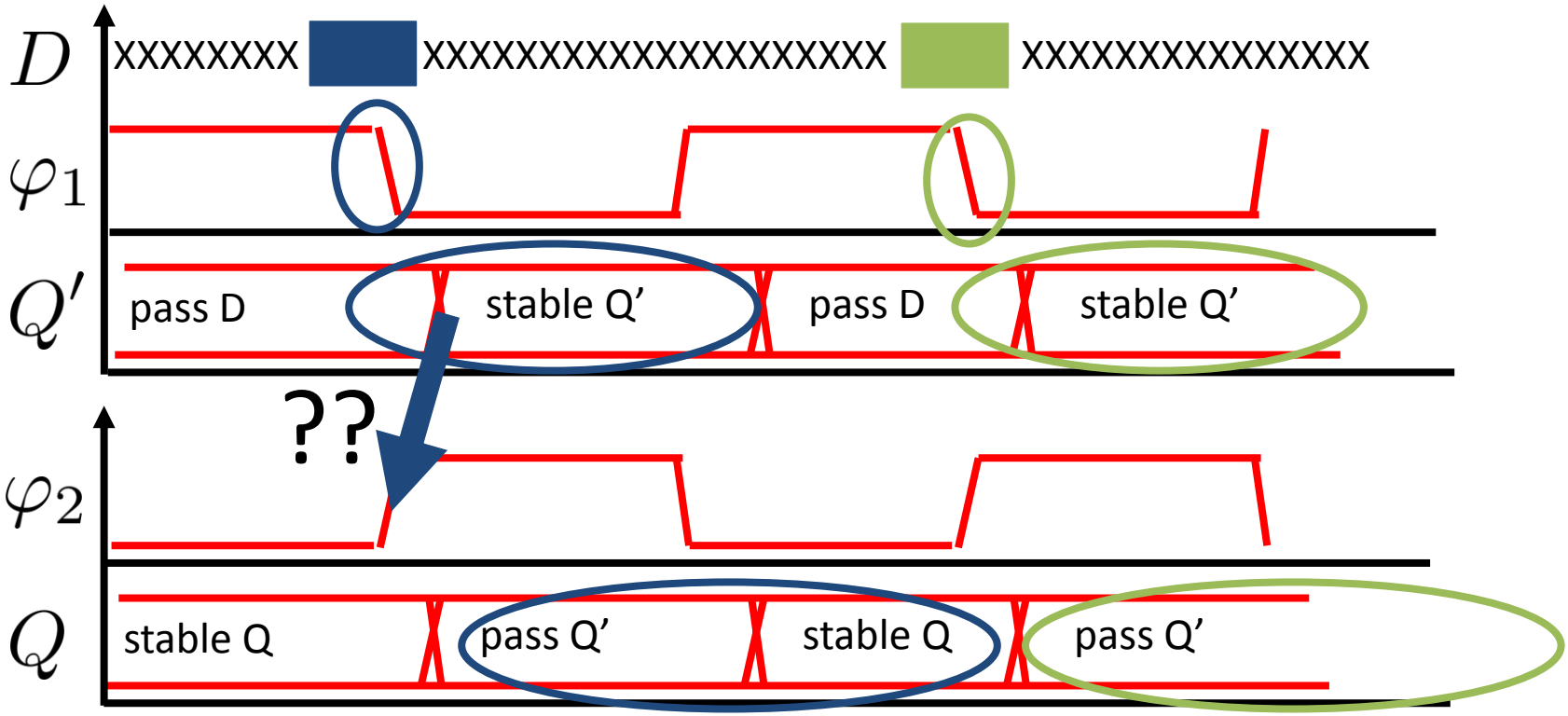
Preventing this...



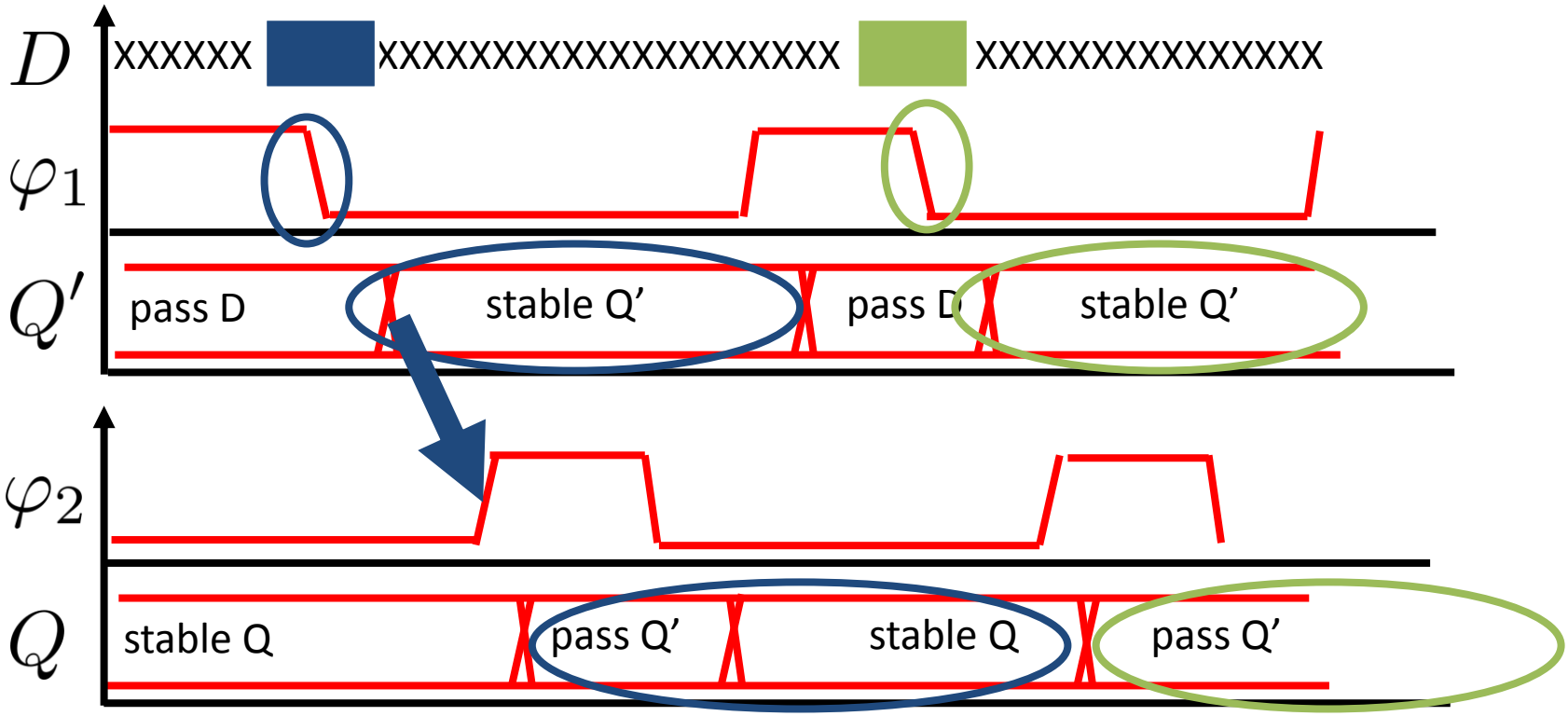
Mind phases



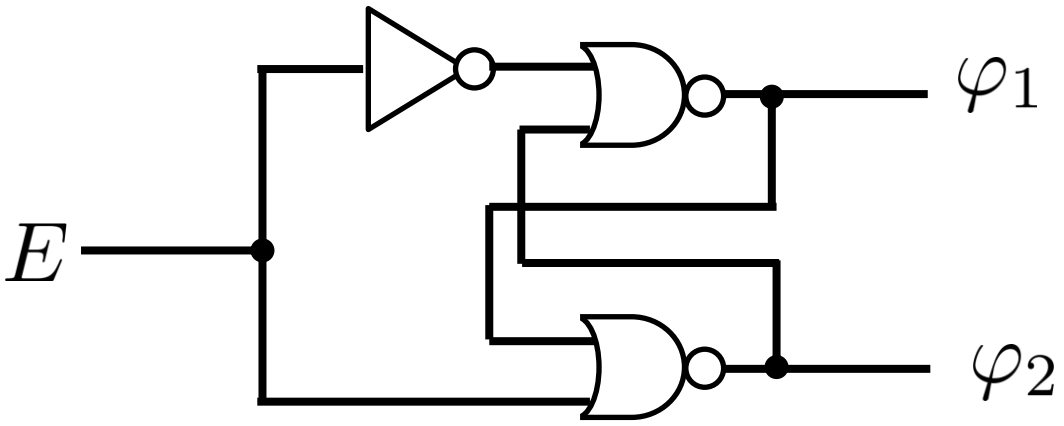
Mind phases


D
xxxxxxxx
xxxxxxxxxxxxxxxxxxxx
xxxxxxxxxxxxxxx
φ1
Q'
pass D
stable Q'
pass D
stable Q'
??
φ2
Q
stable Q
pass Q'
stable Q
pass Q'

Mind phases


D
XXXXXX
XXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXX
φ1
Q'
pass D
stable Q'
pass D
stable Q'
φ2
Q
stable Q
pass Q'
stable Q
pass Q'

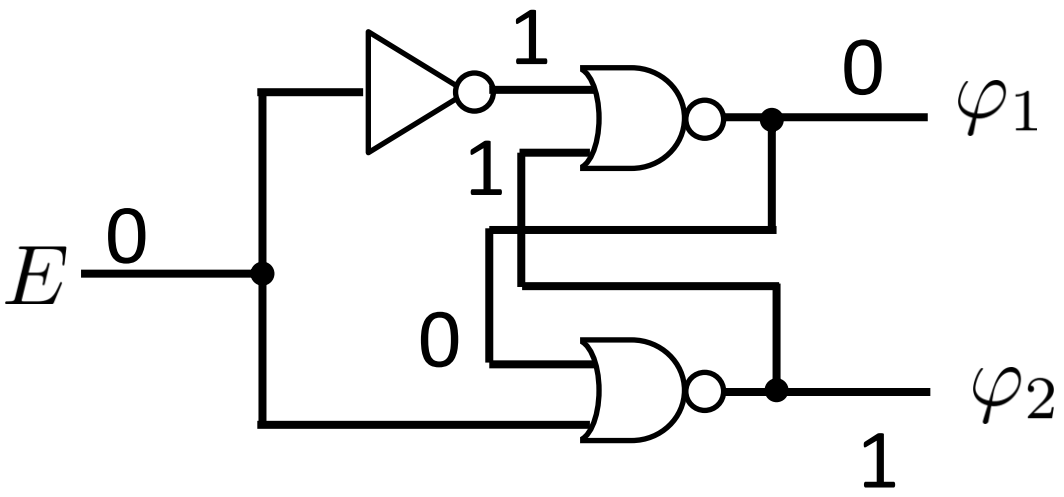
Generate phases (locally)

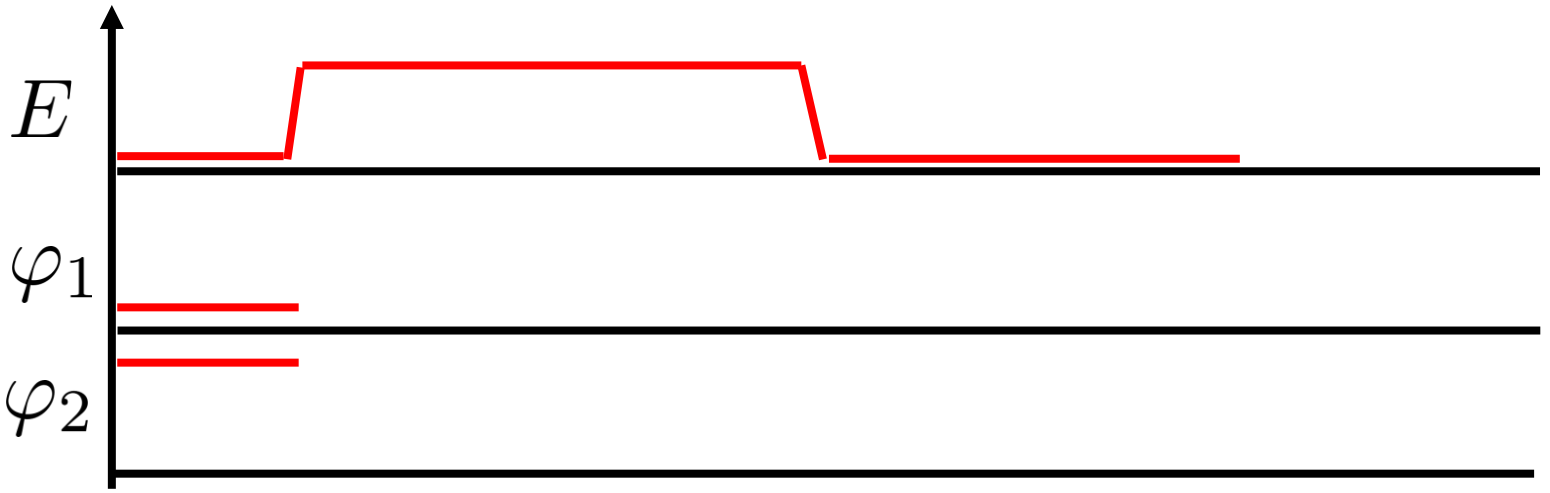


locally since otherwise:

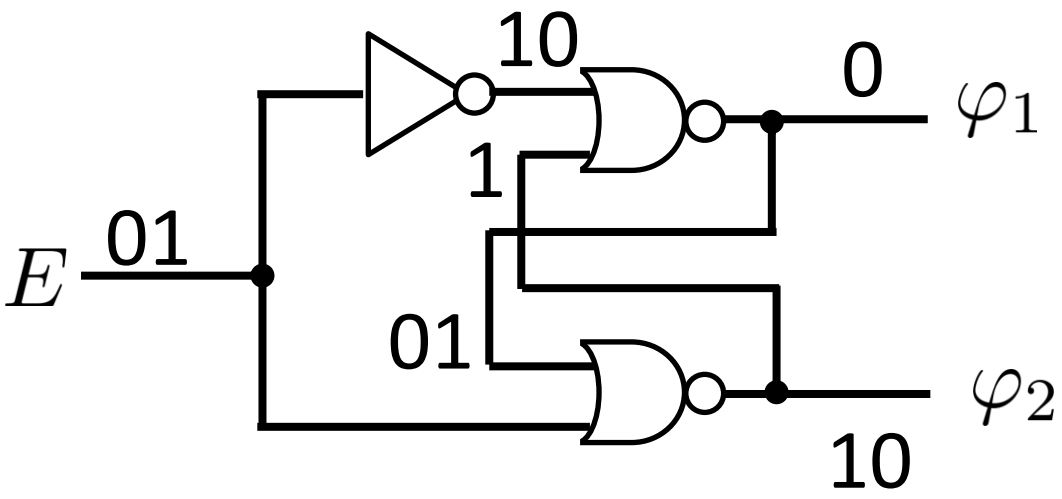
- two signals to distribute
- non-overlap problem, again

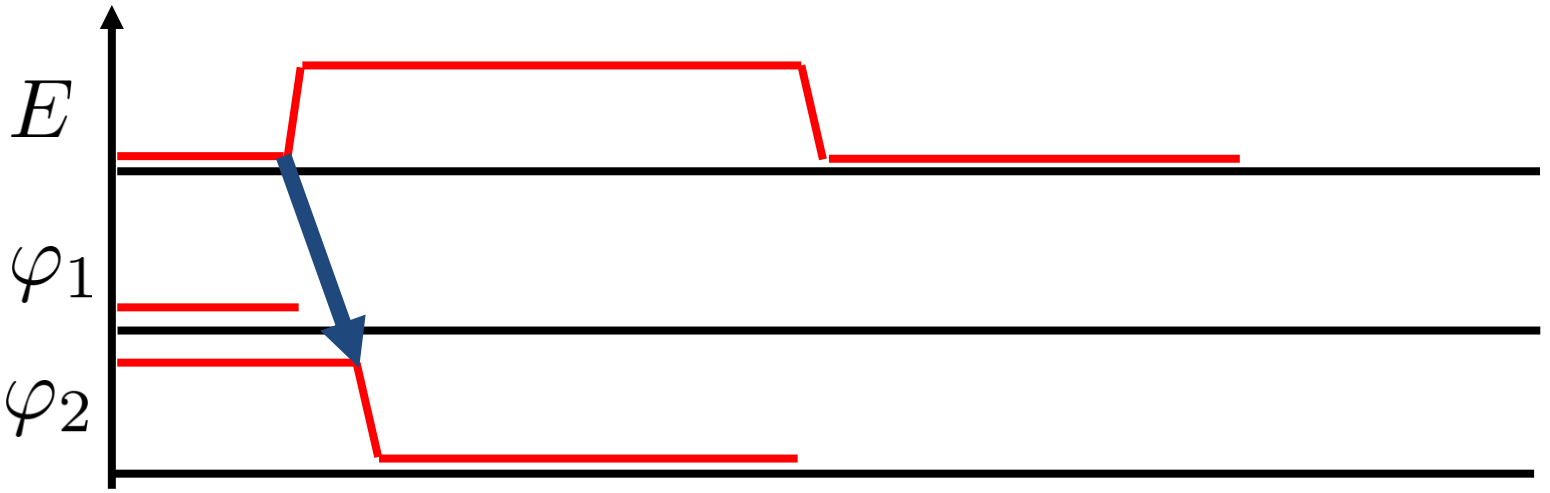
Generate phases (locally)



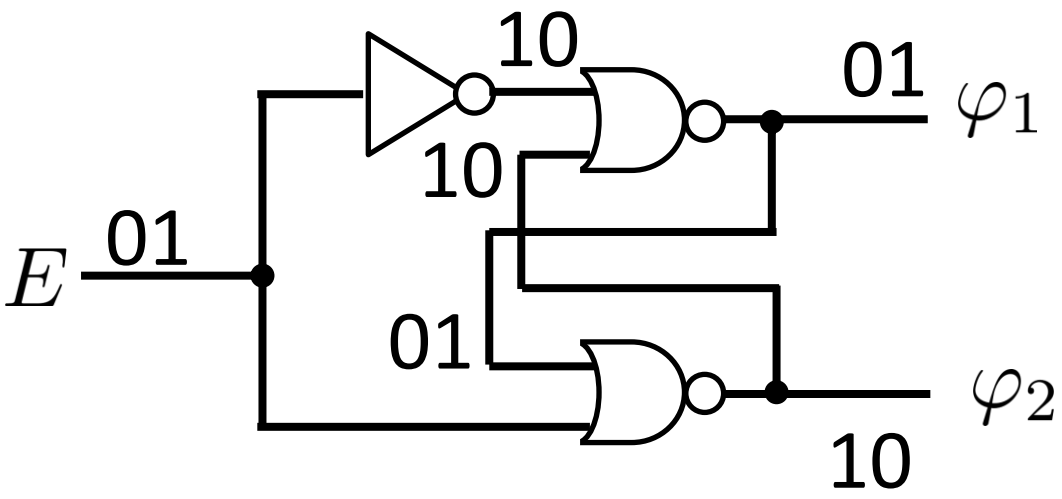


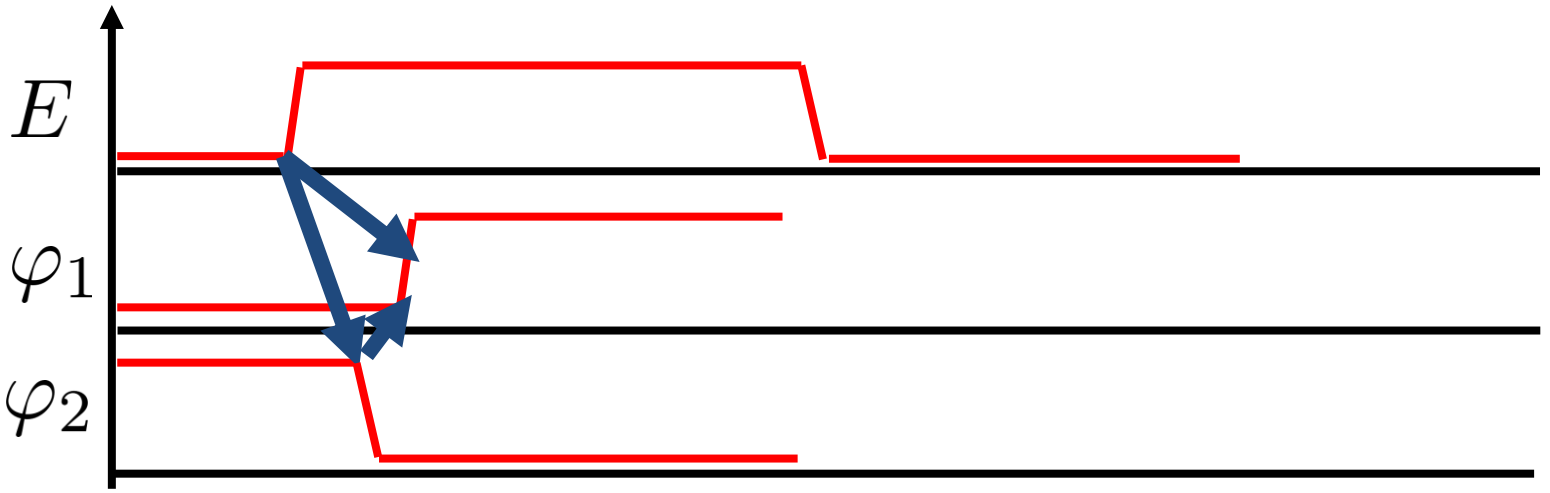
Generate phases (locally)



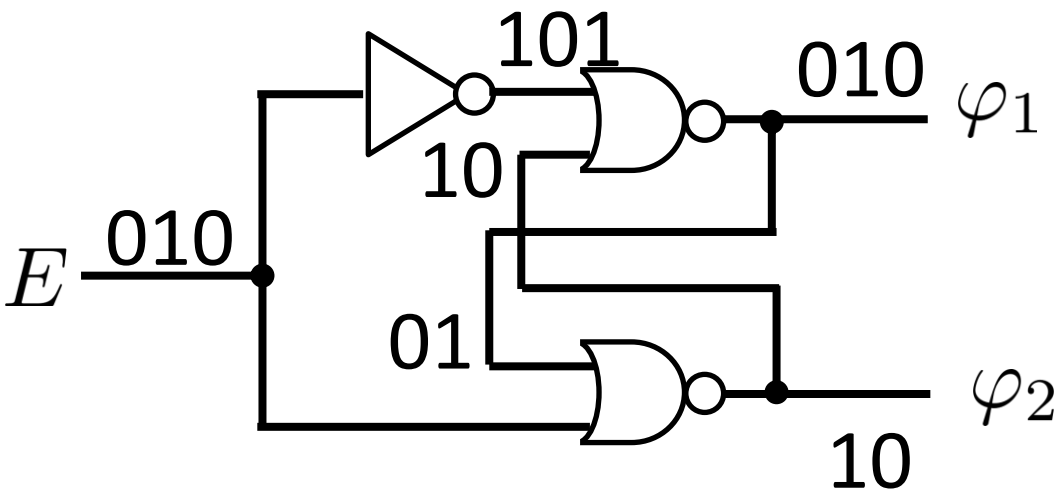


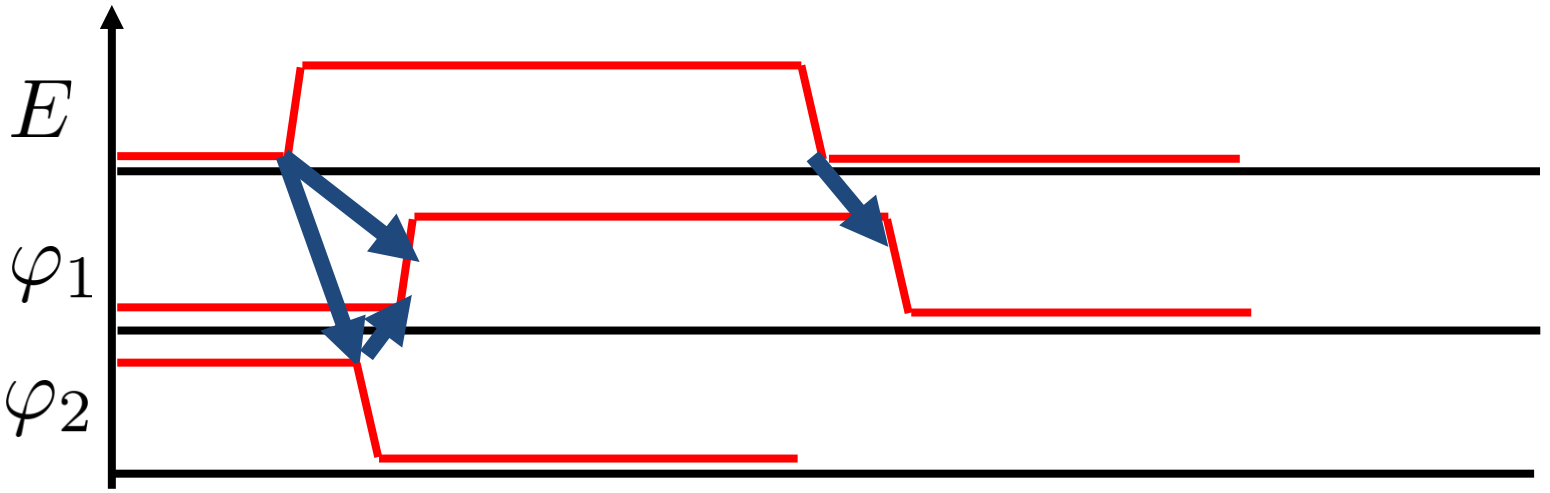
Generate phases (locally)



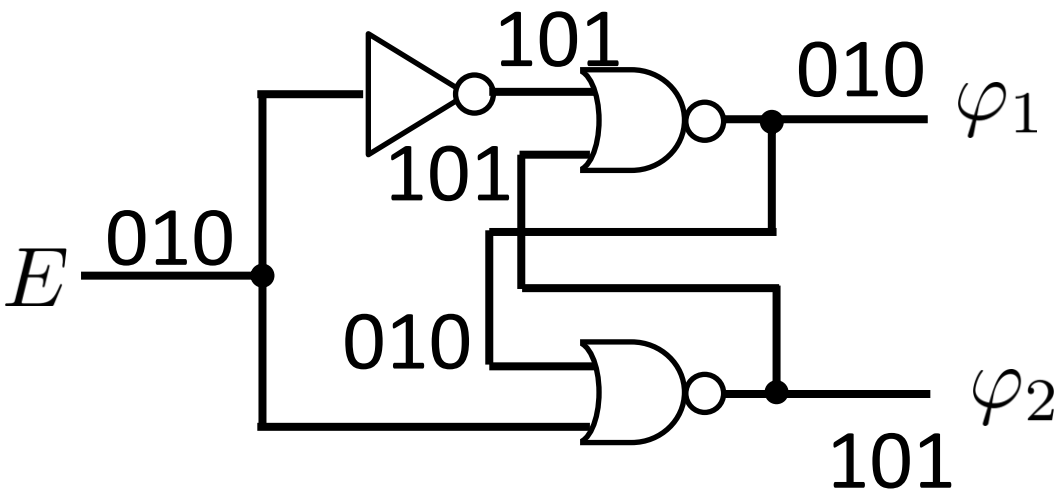


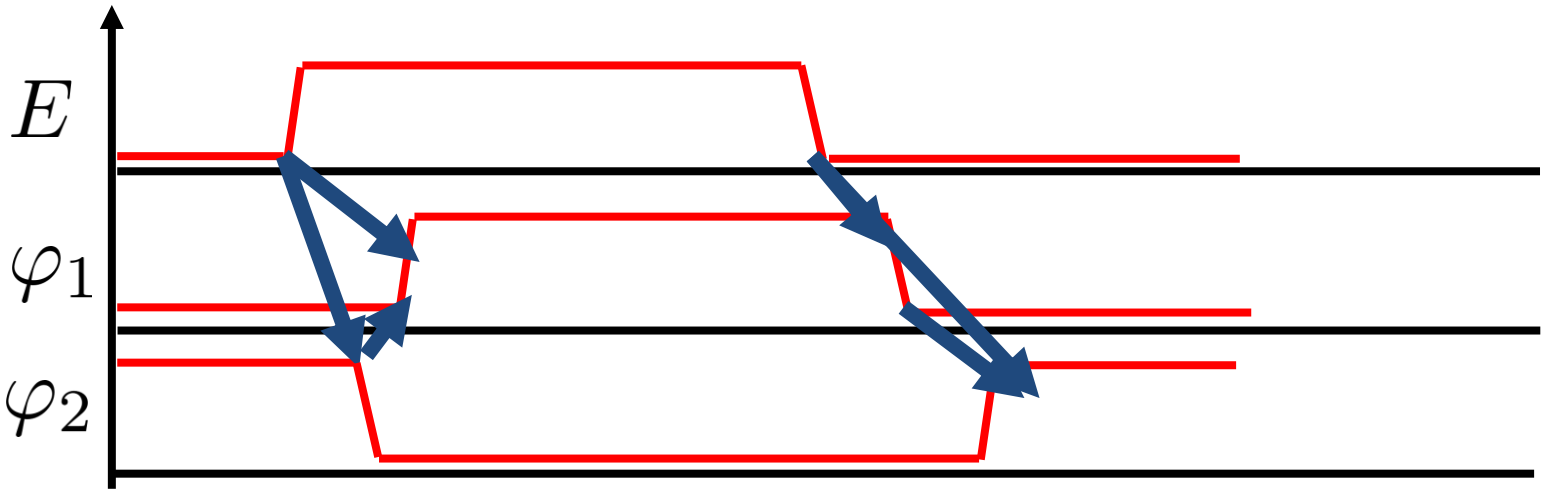
Generate phases (locally)





Generate phases (locally)





Is this static?