Beyond classical chip design
Exercise III

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Ex 11. Prove (A simulates B) $\rightarrow$ (B implements A).

Ex 12 & 13. We have shown that two joined wires are not a wire. In the slides there were a circuit A with a fed-back OR gate with one wire in its feedback and a circuit B that had two wires in its feedback. Assume that initially all ports have value 0. (i) Does A implement B or vice versa? (ii) Does A simulate B or vice versa?

Ex 14 & 15. Assume your combinational logic delay d (in ns) is distributed according to Norm$(1, \sigma)$ with $3\sigma = 0.2$. What is the tradeoff between speed versus reliability with a clockless and with a clocked approach? Let $t(k)$, where $k \geq 1$, be the time the circuit produces its k^{th} data item. For the synchronous circuit $t(k) = kT$, where T is its clock period. For the clockless circuit $t(k) = t(k-1) + d_{req}(k) + d_{ack}(k)$ where $t(0) = 0$ and $d_{req}(k)$ and $d_{ack}(k)$ for all $k \geq 1$ are independently Norm$(1, \sigma)$ distributed. Let $P(\text{fail} \leq k)$ be the probability that a timing violation occurs by the k^{th} data item in the synchronous circuit, i.e., $d_{dat}(k') > T$ for some k' with $1 \leq k' \leq k$.

(i) Compare the two design styles for several mission times (in terms of data items). Assuming that the synchronous circuit is allowed to fail with probability at most 10^{-9} during mission, for which mission times M would you use which design style if you want high expected throughput ($\mathbb{E}(t(M))$)? (ii) What happens if you further decrease $P(\text{fail} \leq k)$ to e.g. 10^{-14}?