Beyond classical chip design
Exercise VI

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Ex 20. (5P) CMOS Inverter. In the slides we presented the characteristics of an nMOS. For simplicity consider the approximation:

$$i_{d,\text{lin}}(V_{DS}, V_{GS}) = 2(V_{GS} - V_{th}) * V_{DS} - V_{DS}^2 \tag{1}$$

$$i_{d,\text{sat}}(V_{DS}, V_{GS}) = (V_{GS} - V_{th})^2 \tag{2}$$

$$i_{d,\text{cutoff}}(V_{DS}, V_{GS}) = 0 \tag{3}$$

$$i_d(V_{DS}, V_{GS}) = \begin{cases} i_{d,\text{cutoff}}(V_{DS}, V_{GS}) & \text{if } 0 > V_{GS} - V_{th} \\ i_{d,\text{sat}}(V_{DS}, V_{GS}) & \text{if } V_{DS} > V_{GS} - V_{th} \\ i_{d,\text{lin}}(V_{DS}, V_{GS}) & \text{otherwise} \end{cases} \tag{4}$$

It gives the drain source current i_d (positive if current flows from drain to source) in relation to V_{DS} and V_{GS}. You can assume $V_{th} = 1V$ for the threshold voltage, here. For the pMOS, all V_{DS}, V_{GS}, V_{th}, i_d are negative. Here we assume $V_{th} = -1V$ and we obtain:

$$i_{d,\text{lin}}(V_{DS}, V_{GS}) = -2(V_{GS} - V_{th}) * V_{DS} - V_{DS}^2 \tag{5}$$

$$i_{d,\text{sat}}(V_{DS}, V_{GS}) = -(V_{GS} - V_{th})^2 \tag{6}$$

$$i_{d,\text{cutoff}}(V_{DS}, V_{GS}) = 0 \tag{7}$$

$$i_d(V_{DS}, V_{GS}) = \begin{cases} i_{d,\text{cutoff}}(V_{DS}, V_{GS}) & \text{if } 0 < V_{GS} - V_{th} \\ i_{d,\text{sat}}(V_{DS}, V_{GS}) & \text{if } V_{DS} < V_{GS} - V_{th} \\ i_{d,\text{lin}}(V_{DS}, V_{GS}) & \text{otherwise} \end{cases} \tag{8}$$

From these equations and the CMOS Inverter circuit derive the static input-output voltage behavior of an inverter. You may do this numerically with your favorite programming language.

1. Plot the input-output voltage characteristics in the steady state.
2. Annotate each point (e.g., by different line style/colors) where with the information in which region nMOS and pMOS are currently operating.
3. Plot the gain over input voltage.
4. Discuss hos the threshold is formed.

Ex 21. (3P) Derive CMOS and pseudo-nMOS circuits for $y = a \wedge b$, $y = (a \wedge b) \vee \neg c$, and $y = (a \wedge b) \vee (\neg a \wedge c) \vee d$. What do observe in terms of circuit size complexity? And how fast do you think these circuits will be if all transistors are the size of those used in the INV?