Beyond classical chip design
Exercise VII

summer term 2015

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Ex 21. (3P) Derive CMOS and pseudo-nMOS circuits for $y = a \wedge b$, $y = (a \wedge b) \vee \neg c$, and $y = (a \wedge b) \vee (\neg a \wedge c) \vee d$. What do you observe in terms of circuit size complexity? And how fast do you think these circuits will be if all transistors are the size of those used in the INV?

Ex 22. (2P) Implement a 2C-Element. Remember that its PRs were: $(a \wedge b) \to y\uparrow$ and $(\neg a \wedge \neg b) \to y\downarrow$. Come up with (i) a dynamic implementation with a V2 statesizer (see slides for terminology), (ii) a ratioed implementation with a V1 statesizer (inverter feedback-loop), and (iii) a V3 combinational implementation. Draw transistor-level circuits for all of them.

Ex 23. (2P) Consider two pass transistors (just nMOS) versus two pass gates (nMOS and pMOS) in series to implement a 2AND. What can you say about the output voltage if the inputs are driven by strong 0 and 1 combinations? How strong/weak will be the output (in terms of V_{dd} and V_{th} and floating (i.e., not connected to either V_{dd} or ground))?