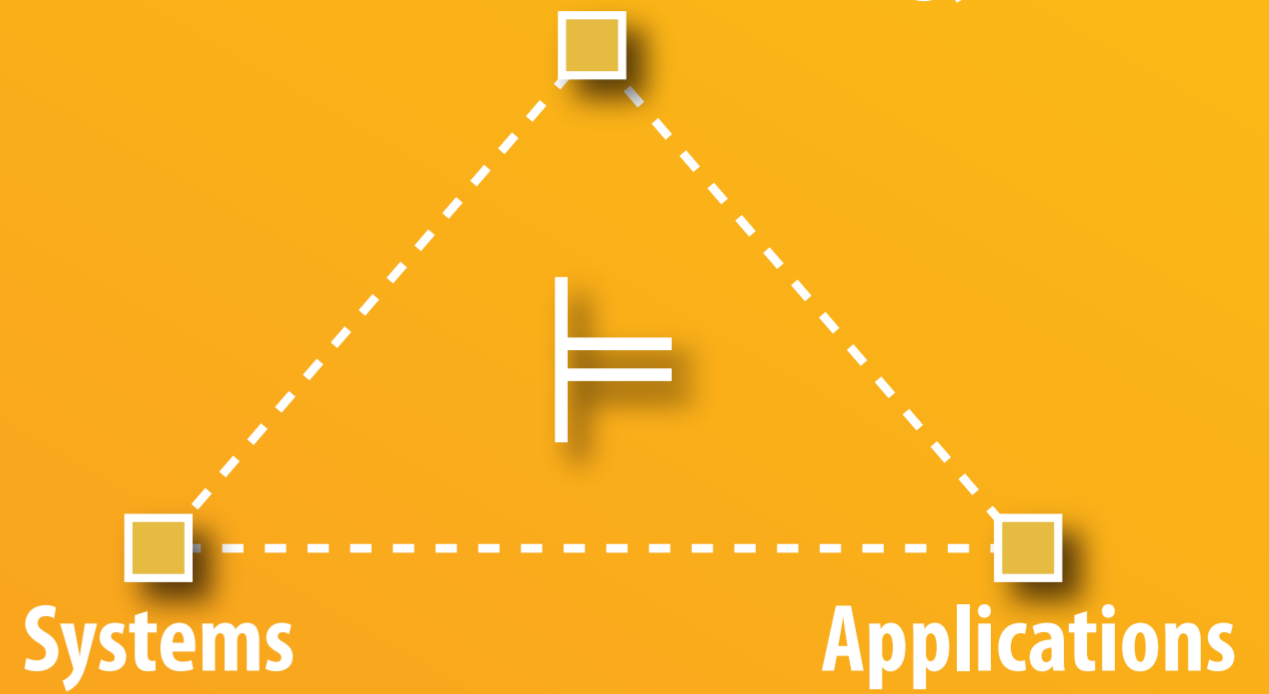Verification Technology

⊨

Systems   Applications

Summer School
on Verification Technology, Systems & Applications

Syntax-Guided Synthesis

Rajeev Alur

Probabilistic Model Checking

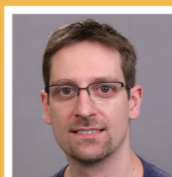**Christel Baier**

Symbolic Computation (Quantifier Elimination)

Hoon Hong

SMT Solvers for Verification and Synthesis

Andrew Reynolds

Introduction to Permission-Based Program Logics

Thomas Wies

July 31–August 4, 2017
Max-Planck-Institut für Informatik
Saarbrücken, Germany

Application Deadline: 2017/06/01
Notification: 2017/06/15

Further Information:
www.mpi-inf.mpg.de/VTSA17